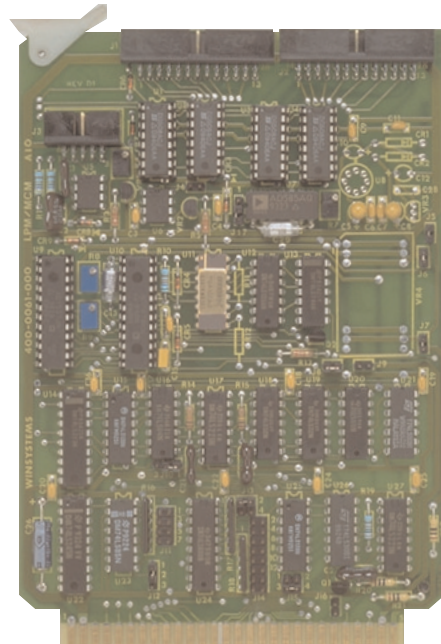


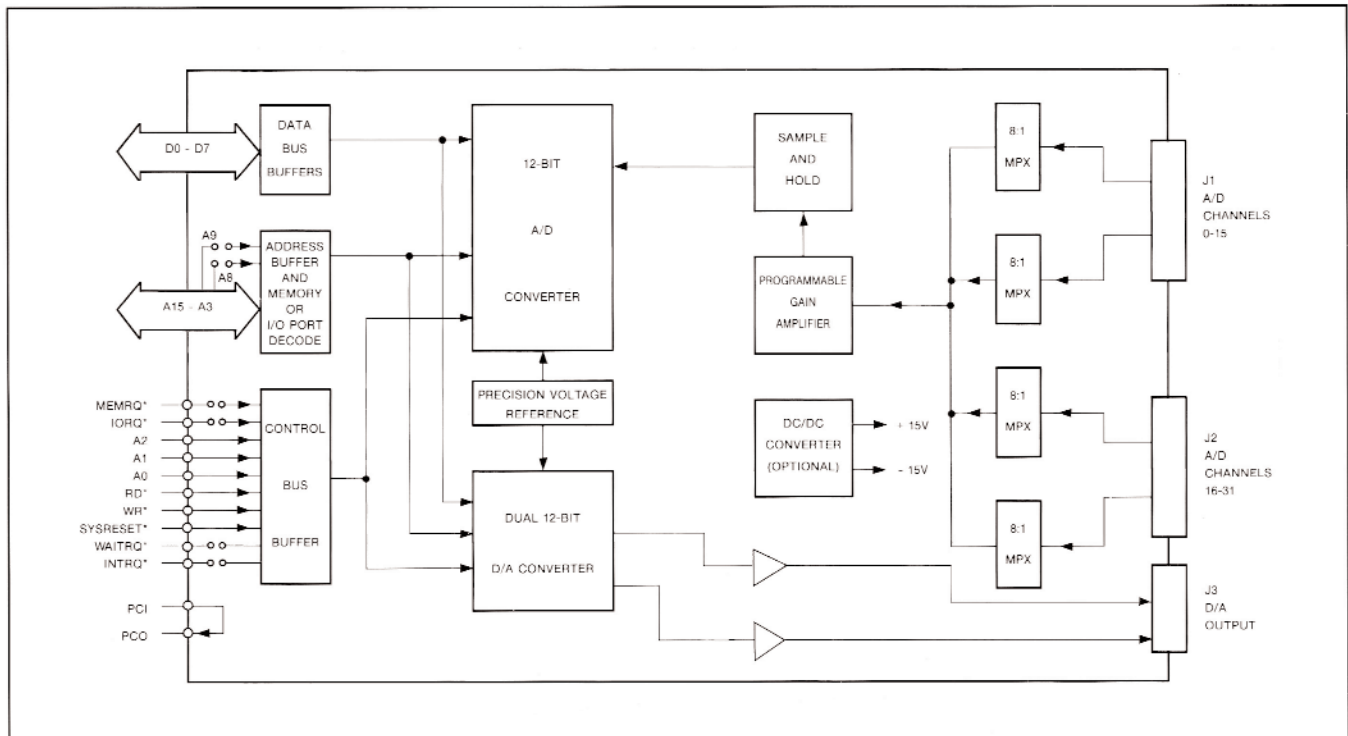
FEATURES

- Up to 32 single ended input channels
- Two analog output channels
- 12-bit resolution for A/D and D/A
- Digitally programmable input amplifier
- Sample and Hold
- 125 uS conversion time
- Interrupt on conversion complete
- Processor independent including V50, V40, V20, 80C88, HD64180, NSC-800, CMOS Z80 and 80C85A
- Jumper selectable Memory or I/O addressing
- Low Cost 8, 16, or 32 channel A/D version available: LPM-AIO-8
- +5V Operation with optional DC Converter
- Available for CMOS STD Bus: LPM-AIO



The LPM/MCM-AIO is a multipurpose 12-bit analog input and output board. It has 32 single ended voltage input channels and 2 voltage output channels. User software programmable gains of 1X, 10X, and 100X are available. The LPM-AIO is a low power CMOS design which will operate over extended temperature ranges.

Installation of an optional DC/DC converters makes the board require +5 volts only. The board is compatible with all STD Bus and CMOS STD Bus CPU cards.



FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-AIO is the CMOS STD Bus versions and the MCM-AIO is the STD Bus versions of these cards. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Wait States - A jumper selectable Wait State generator is on board to generate 1 Wait State for synchronization with fast processors.

Addressing - The card is configured for two modes of addressing: 8/16-bit I/O or 16-bit memory addressing. This provides direct access of up to 64K I/O ports or memory locations by decoding A0 through A15. Typically 8-bit processors will only generate 256 I/O port addresses (A0 - A7). For 808X, NEC "V" series and HD64180 type CPUs, 64K I/O ports can be decoded if required.

On the LPM/MCM-AIO, IOEXP is jumper selectable to be active high, active low, or don't care to double the I/O port addressing range.

For memory mapped CPU's, 64K locations plus MEMEX* are decoded. A jumper selectable active low MEMEX* is supported for additional address qualification.

Address Selection - A total of 16 contiguous addresses are required by the LPM/MCM-AIO and it is jumper selectable on any even 16 port/byte boundary. Programming is very straight forward. The card can be either addressed as successive bytes of memory or a block of I/O ports from a jumper selectable base address.

LPM/MCM-AIO Base Address Map

D7	D6	D5	D4	D3	D2	D1	D0	Byte ADDR
X	PG1	PG0	M4	M3	M2	M1	M0	0
B7	B6	B5	B4	B3	B2	B1	LSB	1
BUSY	IP	X	X	MSB	B10	B9	B8	2
X	X	X	X	X	X	X	X	3
B7	B6	B5	B4	B3	B2	B1	LSB	4
X	X	X	X	MSB	B10	B9	B8	5
B7	B6	B5	B4	B3	B2	B1	LSB	6
X	X	X	X	MSB	B10	B9	B8	7

Notes: 1. The Symbol X means the bit is not used.
2. The BUSY Bit equals "1" during conversion and "0" when Done.

3. The Byte ADDR is fixed but the LPM/MCM-AIO board's boundary address is selectable within the map by on-board jumpers.

Byte 0: MUX ADDRESS/GAIN - The first byte address (0), is used to select any random input channel and the software programmable amplifier's gain by writing to its address. The Write command automatically triggers a timer that sets the Sample and Hold into the "Hold" mode and starts the A/D conversion on the selected channel.

M0 through M4 provide a natural binary select of the 32 channels (0 through 31). The amplifier gain select truth table is as follows:

PG1	PG0	Gain Selected
0	0	1 X
0	1	10 X
1	0	100 X
1	1	Undefined

Byte 1: A/D Low Byte - The 8 lowest order bits of the 12-bit A/D word are available at this address.

Byte 2: A/D High Byte - The 4 highest order bits of the A/D 12-bit word are provided at this address. In addition, the "BUSY" bit provides the status of the A/D converter. The CPU can determine the end-of-conversion cycle by reading this byte. A logic "0" indicates that the conversion is complete and the A/D data is valid and can now be read.

The IP bit represents Interrupt Pending. It indicates the end-of-conversion has been completed and the CPU flagged. The IP bit is cleared by reading the low order data in Byte 1.

Byte 4: DAC0 Low Byte - This byte is written to with the 8 Lowest order bits for the first D/A channel's 12-bit word.

Byte 5: DAC0 High Byte - This byte is written to with the 8 most significant bits for the first D/A channel's 12-bit D/A word.

Byte 6: DAC1 Low Byte - This byte is written to with the 8 lowest order bits for the second D/A channel's 12-bit word.

Byte 7: DAC1 High Byte - This byte is written to with the 8 most significant bits for the second D/A channel's 12-bit D/A word. Writing to this byte commands both D/A converters to update their output with its new value.

Byte 3 and 8 through 15 - These bytes are presently unused by the LPM/MCM-AIO board. Bytes 8 through 15 are reserved but not decoded. Another board in a system can have ports mapped at these locations without redundant addressing conflicts.

Analog Input Section - The LPM/MCM-AIO contains a multiplexer, software programmable gain/fast settling operational amplifier, and a sample-hold circuit. The card accepts up to either 32 single-ended, 0 to +5 volt, unipolar inputs. Total conversion time is 125 μ s.

Multiplexer - The LPM/MCM-AIO card contains up to four 8 channel CMOS Analog Multiplexers with overvoltage protection. They can withstand analog input voltages much greater than the supplies. The multiplexer switches' inputs can withstand 10V greater than either supply with the power off, which eliminates the possibility of damage when supplies are off. Equally important, they can withstand brief input transient spikes which would otherwise require complex external protection networks.

Programmable Gain Amplifier - The outputs of the multiplexers are connected to a PGA-102, precision digitally controlled, Programmable Gain/Fast Settling Operational amplifier. The LPM/MCM-AIO is software programmable for gains of 1, 10, and 100.

Sample and Hold Circuit - The output of the amplifier is connected to a sample-hold circuit which "freezes" the analog input voltage while the A/D converter is performing a conversion. This prevents the voltage from changing while the conversion is in progress. A calibration circuit is provided to trim any error voltages from the amplifier or sample and hold circuitry before reaching the A/D converter.

Analog to Digital Converter - The LPM/MCM-AIO contains an Analog Devices AD7578, 12-bit Successive Approximation A/D converter. It has a conversion time of 100 μ s. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100 μ V. There are no missed codes over the full temperature range. The output code is straight binary.

Digital to Analog Converter - The LPM/MCM-AIO contains an Analog Devices' AD7537 Dual 12-bit DAC. Two independent DACs are on one monolithic chip configured to provide two 0 - 5 volt outputs. The input section is double buffered to allow simultaneous update of both DAC's. A two byte transfer is required to interface an 8-bit CPU byte to the 12-bit D/A.

These registers "memorize" the 12-bit digital word and keeps the D/A converter output constant until it is updated with a new value in one step.

Input Configuration - The analog input channels are wired to two 26-pin, pin-and-socket header connectors, J1 and J2. The first connector inputs channels 0 through 15 and J2 inputs channels 16 through 31. Either flat ribbon cables or discrete wires can be mated to the connectors. The pin-out is identical to the single ended input configuration of the WinSystems' LPM/MCM-A/D12M.

Output Configuration - Each output channel is wired to a 10-pin right angle male connector, J3. Flat ribbon or discrete wires can be connected to it. Alternating ground lines, paired with each output channel's signal line, improves noise immunity and reduces cross-talk.

Interrupts - A/D conversion is begun each time the channel number is written to the board. An end-of-conversion signal can generate a jumper selectable INTRQ* signal on the STD Bus and CMOS STD Bus. This signal also sets an IP flag in bit 6 of Byte 2 for use in a polled mode operation.

DC/DC Power Supply - The card can be operated from \pm 12 VDC or \pm 15 VDC supplied from the STD Bus and CMOS STD Bus. The LPM/MCM-AIO card is offered with an optional DC/DC power supply installed and designated as the LPM/MCM-AIO-DC. This allows the board to operate directly from the microcomputer's +5 volt supply. The DC/DC supply outputs \pm 15 for the analog circuitry. If the analog supply voltages are present in the system, then the extra cost of the optional DC/DC supply is not required.

CMOS STD Bus - The LPM-AIO card is limited to a -25°C lower temperature range because of the A/D converter specifications. WinSystems can optionally populate the board with military range devices to extend it to -40°C. Contact the factory for details.

Standard Configurations - Eight different LPM/MCM-AIO boards are available from WinSystems in different population options. They options include no DACs, DC/DC converter, and fewer input channels. The LPM/MCM-AIO boards without the D/A converters (LPM/MCM-AIO-8, LPM/MCM-AIO-16, LPM/MCM-AIO-32) also do not have the programmable gain amplifier and the sample hold circuitry in order to offer the lowest price card. Contact the

factory if you require a different population other than the ones listed. The standard configurations are as follows:

	AIO CHANNELS	SAMPLE - HOLD	PGA	D/A CHANNELS	+5 ONLY
LPM/MCM-AIO	32	Yes	Yes	2	No
LPM/MCM-AIO-DC	32	Yes	Yes	2	Yes
LPM/MCM-AIO-8	8	No	No	0	No
LPM/MCM-AIO-8-DC	8	No	No	0	Yes
LPM/MCM-AIO-16	16	No	No	0	No
LPM/MCM-AIO-16-DC	16	No	No	0	Yes
LPM/MCM-AIO-32	32	No	No	0	No
LPM/MCM-AIO-32-DC	32	No	No	0	Yes

SPECIFICATIONS

Electrical

Analog Input

Number of Channels: Up to 32 single-ended
 Input Impedance: greater than 100 Megohms
 Input Overvoltage: $\pm 10V$ (with power off)
 Input Ranges: 0 to +5 V (with programmable gain)
 Coding: straight binary (unipolar)
 Resolution: 12-bits
 Nonlinearity: 1 LSB
 Conversion Time: 125 microseconds (includes sample-hold time and slew rates for the amplifier and multiplexers)

Analog Output

Number of Channels: 2 (LPM/MCM-AIO)
 D/A Resolution: 12-bits
 Coding: Straight Binary
 Output Voltage: 0 to +5 volts
 Differential Nonlinearity: ± 1 LSB
 Relative Accuracy: ± 1 LSB
 Output Settling Time: 5 μ s

Power Requirements

LPM/MCM-AIO configured with 32 input A/D channels, amplifier, sample-hold and 2 D/A channels

Without DC to DC Converter
 +5 VDC $\pm 5\%$ at 5 mA (typ.)
 +12/15 VDC $\pm 5\%$ 44 mA (typ.)
 -12/15 VDC $\pm 5\%$ 22 mA (typ.)

With DC to DC Converter
 +5 VDC $\pm 5\%$ at 200 mA (typ.)

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

STD Bus: 56-pin dual 0.125 inch centers
 Input: Two 26-pin dual on 0.100" grid
 Output: One 12-pin dual on 0.100" grid
 Jumpers: 0.025" square posts

Environmental

Operating Temperature:
 LPM-AIO -25°C to +85°C
 MCM-AIO 0°C to +65°C
 Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-AIO	12-bit, 32 channel analog input and 2 channel analog output card
LPM-AIO-DC	12-bit analog input/output board with DC/DC converter for single +5 VDC operation
LPM-AIO-8	Low cost 12-bit A/D with 8 S.E inputs
LPM-AIO-8-DC	LPM-AIO-8 with DC/DC converter (+5V only)
LPM-AIO-16	Low cost 12-bit A/D with 16 S.E inputs
LPM-AIO-16-DC	LPM-AIO-16 with DC/DC converter (+5V only)
LPM-AIO-32	Low cost 12-bit A/D with 32 S.E inputs
LPM-AIO-32-DC	LPM-AIO-32 with DC/DC converter (+5V only)
MCM-AIO	12-bit, 32 channel analog input and 2 channel analog output card
MCM-AIO-DC	12-bit analog input/output board with DC/DC converter for single +5 VDC operation
MCM-AIO-8	Low cost 12-bit A/D with 8 S.E inputs
MCM-AIO-8-DC	LPM-AIO-8 with DC/DC converter (+5V only)
MCM-AIO-16	Low cost 12-bit A/D with 16 S.E inputs
MCM-AIO-16-DC	LPM-AIO-16 with DC/DC converter (+5V only)
MCM-AIO-32	Low cost 12-bit A/D with 32 S.E inputs
MCM-AIO-32-DC	LPM-AIO-32 with DC/DC converter (+5V only)

