

# **OPERATIONS MANUAL LPM/MCM-A/D12**

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**REVISION HISTORY**

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## Section 1

# General Information

### Features

- STD Bus Compatible
- 12 Bit A/D
- 16 Single ended or 8 differential channels
- Interrupt on conversion
- 5 Input Voltage Ranges
- Optional DC/DC Convertor for +5V operation

### Additional Features: *LPM-A/D12*

- Extended Temperature Operations: -20°C. to 85°C.
- All CMOS for Low Power Operation

### General Description

■ The LPM/MCM-A/D12 is a 12 bit analog to digital converter board designed for the STD BUS. The LPM/MCM-A/D12 offers the user 16 single ended or 8 differential channels with five jumper selectable input voltage ranges. The LPM/MCM-A/D12 can be operated from +/- 12 VDC or +/- 15 VDC supplied from the STD BUS or from +5 VDC only with an optional on board DC/DC converter. (NOTE: For +/- 12 VDC operation, the input range is limited to +/- 5 VDC) Lower input voltage ranges can be accommodated by installing a single resistor to increase the gain of the instrumentation amplifier.

The LPM/MCM-A/D12 is designed with the Analog Devices ADC-80 analog to digital convertor. The ADC-80 is a 12 bit ADC that has a 25 us conversion time. The ADC-80 produces straight binary for unipolar voltages, and offset binary for bipolar voltages. In addition, the MSB can be complemented to produce 2's complement.

The 16 channels for singled ended operation or 8 channels for differential operation is implemented by the use of two 8 channel CMOS switches. These switches can withstand +/- 20 V with the power off, or +/- 32 V with the power on. Digital inputs for selecting a particular channel are controlled by a 4 bit latch that holds the channel number for conversion. A new conversion is begun each time that a new channel number is written into the latch.

The input multiplexers feed the instrumentation amplifier. The LPM/MCM-A/D12 uses the Burr-Brown INA-101 monolithic instrumentation amplifier for high input impedance and common mode rejection. The input of the instrumentation amplifier can be jumpered for single ended or differential operation.

The output of the ADC is controlled by I/O ports that are interfaced to the STD BUS. One write only port is used to output the channel number and begin the conversion. Two read ports are used to allow the 12 bits from the ADC, and status information to be read. A complete conversion can be detected by polling the BUSY flag or by enabling interrupts on the LPM/MCM-A/D12. When the conversion is complete, the LPM/MCM-A/D12 will interrupt the CPU and the data can then be read out by the use of an interrupt service routine. The interrupt is cleared on the LPM/MCM-A/D12 by reading the data.

## Specifications

### Analog Input

- Number of Channels: 16 single ended or eight differential
- Input Impedance: 100 megohm
- Input Overvoltage: +/- 35V (+/- 20V with power off)
- Input Ranges: +/- 2.5V, +/- 5V, 0-5V with +/- 12V supplies  
+/- 2.5V, +/-5V, +/- 10V, 0-5V, 0-10V with +/- 15V
- Coding, unipolar: straight binary
- Coding, bipolar: offset binary, 2's complement
- Resolution: 12 bits
- Nonlinearity: +/- 1/2 LSB
- Differential Nonlinearity: +/- 1/2 LSB
- Gain Error: Adjustable to zero
- Offset or Zero Error: Adjustable to zero
- Accuracy: +/- .03 % FSR
- Conversion Time: 75 US

### Interface

- All address, data, and control lines are CMOS/STD BUS compatible

### Connector

- 56 pin dual 0.125 inch centers

### Power Requirements (LPM-A/D12)

- Without DC to DC Convertor
  - +5 VDC +/- 10% at 75 mA
  - +12/15 VDC +/- 5% 35 mA.
  - 12/15 VDC +/- 5% 35 mA.
- With DC to DC Convertor
  - +5 VDC +/- 10% at 300 mA.

### Power Requirements (MCM-A/D12)

- Without DC to DC Convertor
  - +5 VDC +/- 5% at 400 mA
  - +12/15 VDC +/- 5% 35 mA.
  - 12/15 VDC +/- 5% 35 mA.
- With DC to DC Convertor
  - +5 VDC +/- 10% at 600 mA.

### Operating Temperature

- -20°C. To +85°C. (LPM-A/D12)
- 0°C. TO +60°C. (MCM-A/D12)

**Card Dimensions**

- Height 6.5 inches
- Width 4.48 inches
- Thickness .50 inches

## Section 2

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# User Options

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### I/O Address Decoder

■ The LPM/MCM-A/D12 is an I/O mapped device, and uses one write only I/O port and two read only ports. A jumper selectable address decoder is used so that several I/O boards can be used in a system without data bus contention problems. The LPM/MCM-A/D12 can be strapped for sixteen different I/O addresses by the use of jumper block J6. These I/O addresses are shown in Table 2-1 with the strapping for J6. See Figure 2-4 for the LPM/MCM-A/D12 I/O map.

**Table 2-1**  
**I/O Address Decoder Strapping, J6**

HEX	0-2	4-6	8-A	C-E	10-12	14-16
	10—02	10—02	10—02	10—02	10—02	10—02
	30—04	30—04	30—04	30—04	30 04	30 04
	50—06	50—06	50 06	50 06	50—06	50—06
	70—08	70 08	70—08	70 08	70—08	70 08

HEX	18-1A	1C-1E	20-22	24-26	28-2A	2C-2E
	10—02	10—02	10 02	10 02	10 06	10 02
	30 04	30 04	30—04	30—04	30—04	30—04
	50 06	50 06	50—06	50—06	50 06	50 06
	70—08	70 08	70—08	70 08	70—08	70 08

HEX	30-32	34-36	38-3A	3C-3E
	10 02	10 02	10 02	10 02
	30 04	30 04	30 04	30 04
	50—06	50—06	50 06	50 06
	70—08	70 08	70—08	70 08

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➔ *Address bits A0,A1,A6, and A7 are decoded on the board.*

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## Analog Input Connector Pin-Out

- The analog inputs to the LPM/MCM-A/D12 are made through connector J1 located at the top of the board. Table 2-2 shows the pin out for the 16 single ended channels and the eight differential channels.

**Table 2-2**  
**J1 Pin-Out for Single Ended or Differential Operation**

J1

Differential	Single Ended	Pin #		Single Ended	Differential
Chan 0 (+)	Chan 0	1	14	Chan 8	Chan 0 (-)
Chan 1 (+)	Chan 1	2	15	Chan 9	Chan 1 (-)
Analog Ground		3	16	Analog Ground	
Chan 2 (+)	Chan 2	4	17	Chan 10	Chan 2 (-)
Analog Ground		5	18	Analog Ground	
Chan 3 (+)	Chan 3	6	19	Chan 11	Chan 3 (-)
Analog Ground		7	20	Analog Ground	
Chan 4 (+)	Chan 4	8	21	Chan 12	Chan 4 (-)
Analog Ground		9	22	Analog Ground	
Chan 5 (+)	Chan 5	10	23	Chan 13	Chan 5 (-)
Analog Ground		11	24	Analog Ground	
Chan 6 (+)	Chan 6	12	25	Chan 14	Chan 6 (-)
Chan 7 (+)	Chan 7	13	26	Chan 15	Chan 7 (-)

## Single Ended and Differential Input Configurations

- The LPM/MCM-A/D12 can be configured for single ended or differential operation. The single ended mode of operation allows the maximum number of input channels (16), while the differential mode of operation only allows eight. The advantage of the differential mode is that it offers the highest noise rejection and common mode rejection ratio (CMMR) for low level data acquisition applications. Figure 2-1 shows the strapping for jumper blocks J2 and J3 for single ended operation. Figure 2-2 shows the strapping for differential operation.

**Figure 2-1**  
**J2,J3 Strapping for Single Ended Operation**



**Figure 2-2**  
**J2,J3 Strapping for Differential Operation**



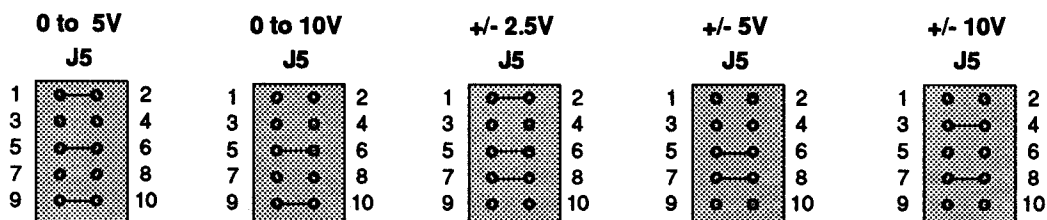
**NOTE :** When using the differential mode of operation, the (+) and (-) inputs must have a bias return path to ground or else the instrumentation amplifier will saturate. This requirement can be satisfied by installing 1 megohm resistors in the user installable resistor locations R15 and R16. See the schematic diagram in the Appendix.

## Input Ranges

■ The LPM/MCM-A/D12 has five different input voltage ranges controlled by jumper block J5. Figure 2-3 shows the strapping for J5 vs the input voltage ranges.

➔ For input voltage ranges above 5 volts, the LPM/MCM-A/D12 must be operated with +/- 15 VDC supplies, otherwise non-linear operation will result.

**Figure 2-3**  
J5 Input Voltage Jumpers



## Software Interface

■ The LPM/MCM-A/D12 is very simple to use. For example, assume that the LPM/MCM-A/D12 is strapped for I/O addresses 0-2 HEX, and single ended operation. To begin a conversion, the channel number is output to the "MUX Address & Conversion Command" register located at the base address. This will cause the multiplexers to switch to the specified channel, the BUSY bit located in input port bit 7 (MSB) to be set high indicating that a conversion is in progress. Approximately 75  $\mu$ s later, the BUSY bit will be reset indicating that the conversion is complete, and data can be read from input ports 1 and 2. Input port 1 contains the least significant byte and the lower four bits of input port 2 contains the most significant four bits. Figure 2-4 shows the I/O port map for the previous example.

**Figure 2-4**  
I/O Port Map for LPM/MCM-A/D12

I/O Address	D7	D6	D5	D4	D3	D2	D1	D0	Function	Operation
00aaaa00	X	X	X	X	M3	M2	M1	M0	MUX Address & Conv CMD	Write
00aaaa01	B7	B6	B5	B4	B3	B2	B1	B0	Lower ADC Byte	Read
00aaaa10	Busy	INT	X	X	B11	B10	B9	B8	Upper ADC Byte & Status	Read

- 
- ➔ 1. I/O address bits "aaaa" are programmable by the use of jumper block J6.

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  - ➔ 2. "X" bits are don't cares.

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  - ➔ 3. Busy bit is a "1" while a conversion is in progress and a "0" when finished.

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  - ➔ 4. The INT bit is set to a "1" when a conversion is completed, and will remain set until the lower ADC byte is read. The INT bit can be used by an interrupt service routine to determine if the LPM/MCM-A/D12 generated an interrupt to the CPU card.

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  - ➔ 5. Writing the multiplexer number to I/O port address 00aaaa00 will set the input channel and start a conversion.

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  - ➔ 6. A SYSTEM RESET will clear BUSY and INT.

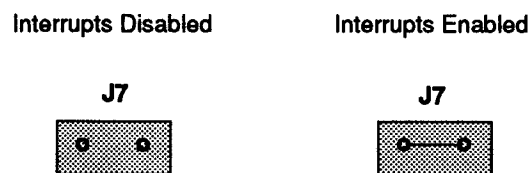
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  - ➔ 7. The MSB bit can be inverted by connecting J4 1 to 2. The LPM/MCM-A/D12 is shipped with J4 3 to 4.

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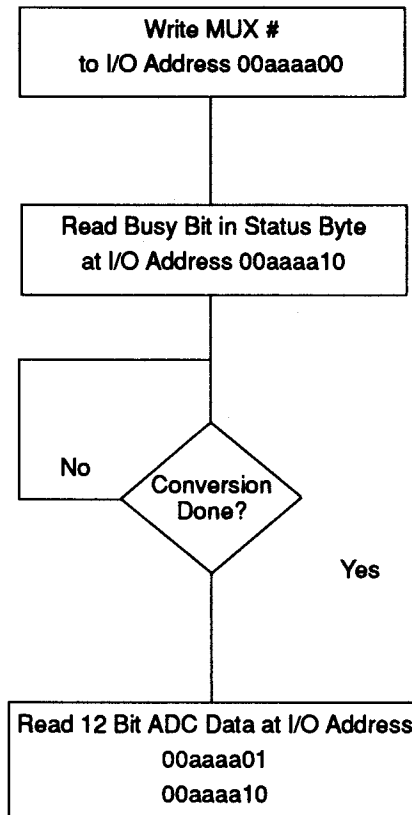
■ The LPM/MCM-A/D12 is capable of generating an interrupt on the completion of a conversion cycle. The interrupt for the LPM/MCM-A/D12 is enabled by jumper block J7. See figure 2-5 below. At the end of a conversion cycle, the LPM/MCM-A/D12 will set the INT bit, and if enabled by J7, will activate the INTRQ line (PIN #44) on the STD BUS. Both the INT bit in the status register and the INTRQ line on the STD BUS will remain active until data is read from the lower ADC input port. The INT bit in the status register can be used by an interrupt service routine to determine if the LPM/MCM-A/D12 generated an interrupt. See flow chart in figure 2-7 for interrupt service routine.

**Figure 2-5**  
**Interrupts**

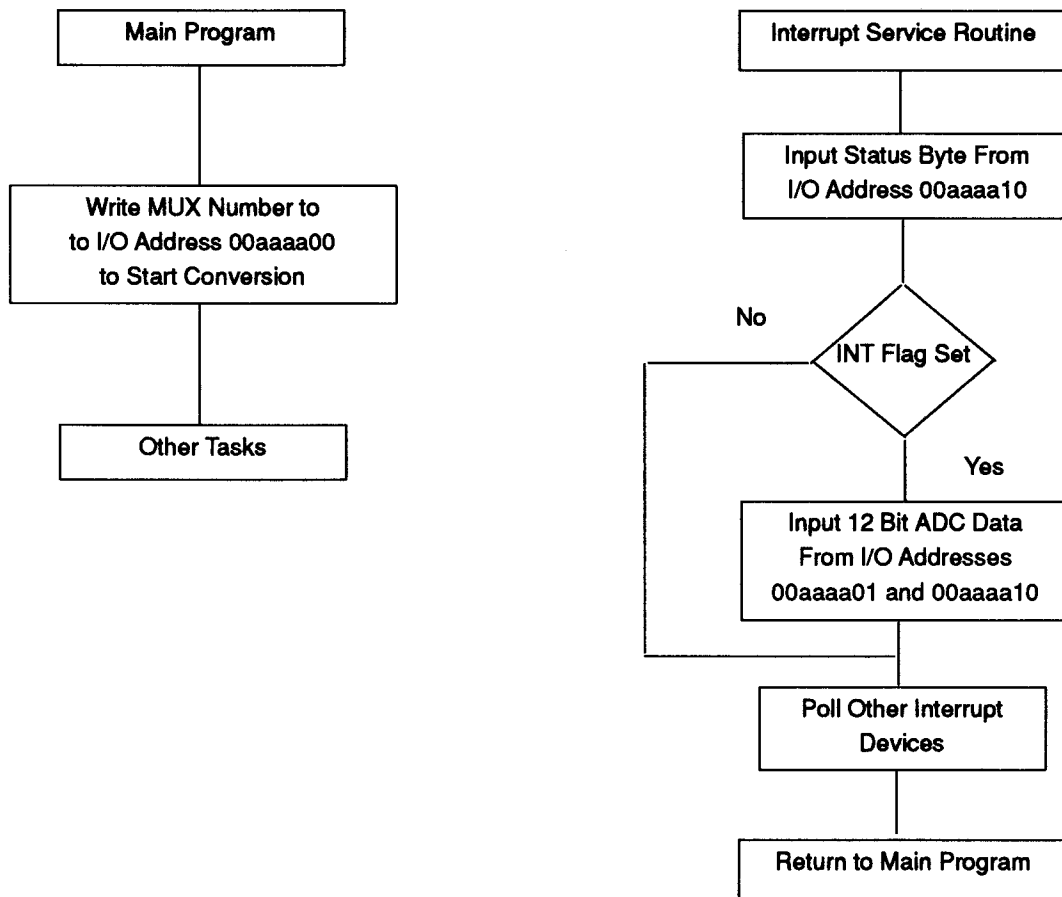


■ Figure 2-6 shows a flow chart for a "polled mode" software interface while figure 2-7 shows an "interrupt mode" interface for analog to digital conversion using the LPM/MCM-A/D12.

**Figure 2-6**  
**LPM/MCM-A/D12 Polled Mode for A/D Conversion**



**Figure 2-7**  
**Flow chart for Interrupt Mode**



### Calibration Procedures

■ The LPM/MCM-A/D12 is calibrated at the factory for the 0-5V range of operation. When switching to another input range, a slight adjustment may be necessary. The following procedure is given to calibrate the LPM/MCM-A/D12 for any input range. Table 2-3 shows the output coding for the various input ranges.

#### Calibration Procedure

1. Select the desired input voltage range as shown in section 2.4. Use one of the routines as described section 2.5, software interface to start and readout a conversion.

2. Zero and offset adjustment. (TRIMPOT R6): Apply a voltage source between the selected analog channel and ground. Adjust the output of the voltage source to +1/2 LSB. Adjust the zero trimming potentiometer R6 so that the output code flickers equally between 000 HEX and 001 HEX for unipolar operation and 800 HEX and 801 HEX for the bipolar mode.

3. Full scale adjustment. (TRIMPOT R5): Change the output of the voltage source for +FS-1 1/2 LSB. Adjust the gain trimming potentiometer R5 so that the output code flickers equally between FFE HEX and FFF HEX.

**Table 2-3  
Output Coding**

Input Voltage Range				Coding		
Unipolar				Straight Binary		
	0 to 10V	0 to +5V		MSB		LSB
+FS-1 LSB	+9.9976	+4.9988		1111	1111	1111
+1/2 FS	+5.0000	+2.5000		1000	0000	0000
+1 LSB	+0.0024	+0.0012		0000	0000	0001
Zero	0.0000	0.0000		0000	0000	0000
Bipolar				Offset Binary*		
	+/- 10V	+/- 5V	+/- 2.5V	MSB		LSB
+FS-1 LSB	+9.9951	+4.9976	+2.4988	1111	1111	1111
+1/2 FS	+5.0000	+2.5000	+1.2500	1100	0000	0000
+1 LSB	+0.0049	+0.0024	+0.0012	1000	0000	0001
Zero	0.0000	0.0000	0.0000	1000	0000	0000
-FS-1 LSB	-9.9951	-4.9976	-2.4988	0000	0000	0001
-FS	-10.0000	-5.0000	-2.5000	0000	0000	0000

\* For 2's complement: Connect J4 1-2, Disconnect J4 3-4

### Instrumentation Amplifier Gain

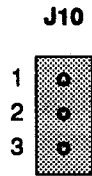
■ The INA-101 (U4) is a high accuracy, multistage, integrated circuit instrumentation amplifier designed for signal conditioning applications. The gain of the instrumentation amplifier U4 is set by resistor, R1 with a gain equation of:

$$G = 1 + (40K/R1)$$

The LPM/MCM-A/D12 is shipped from the factory with R1 open for a unity gain configuration.

## /IOEXP

■ The LPM/MCM-A/D12 can be jumpered so that /IOEXP will enable or disable the board. When /IOEXP is enabled on the LPM/MCM-A/D12, the LPM/MCM-A/D12 will be selected when /IOEXP is low and the selected I/O address for the LPM/MCM-A/D12 is decoded. /IOEXP is controlled by the jumper block J10.

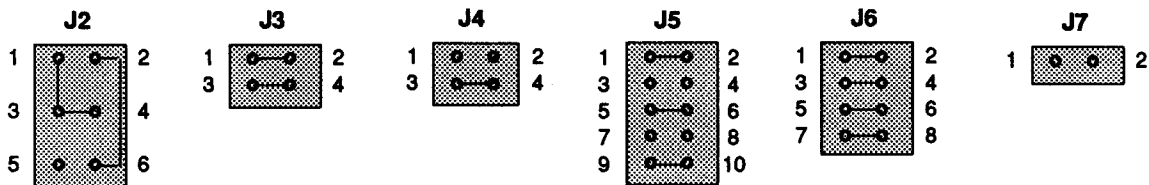


To enable /IOEXP: Connect J10 2-3      To disable /IOEXP: Connect J10 1-2

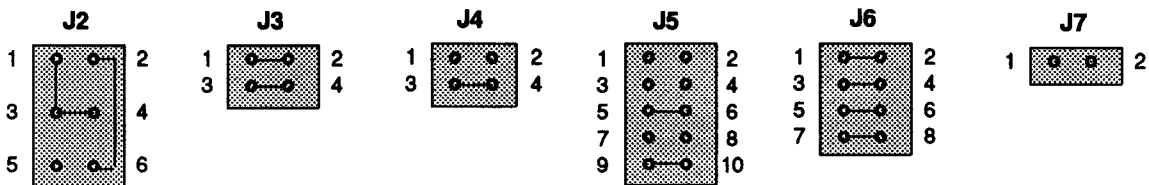
## Examples

■ This section is provided to give some common application examples of the LPM/MCM-A/D12.

- Example #1
  - Configuration:
    - Number of input channels: 16 single ended
    - Input voltage range: 0-5V
    - I/O address: 0-2 HEX



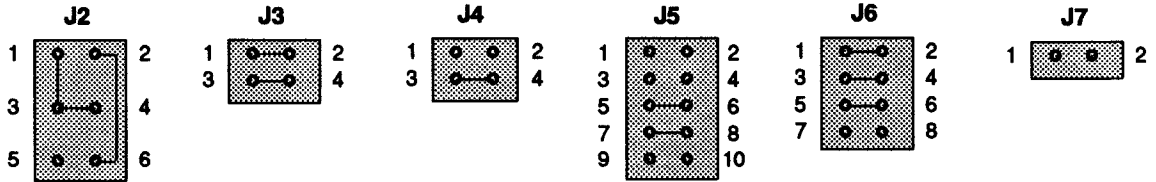
- Example #2
  - Configuration:
    - Number of input channels: 16 single ended
    - Input voltage range: 0-10V (REQUIRES +/- 15 VDC SUPPLIES)
    - I/O address: 0-2 HEX



- Example #3

- Configuration:

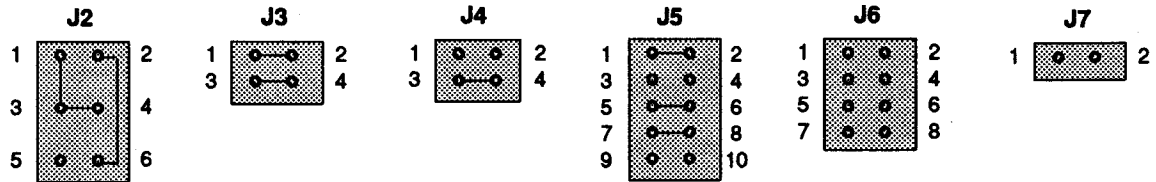
- Number of input channels: 16 single ended
    - Input voltage range: +/- 5 V
    - I/O address: 4-6 HEX



- Example #4

- Configuration:

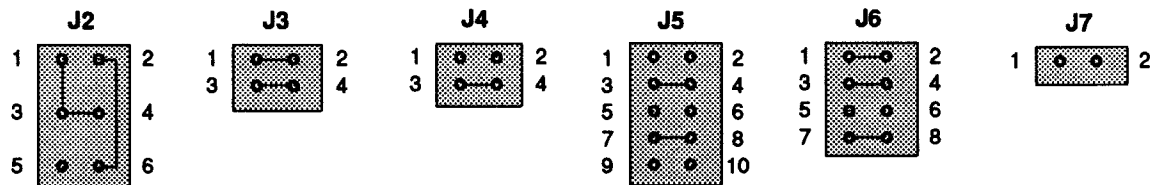
- Number of input channels: 16 single ended
    - Input voltage range: +/- 2.5 V
    - I/O address: 3C-3D HEX



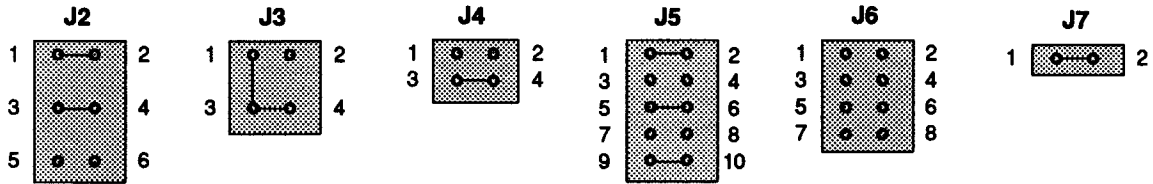
- Example #5

- Configuration:

- Number of input channels: 16 single ended
    - Input voltage range: +/- 10 V (Requires +/- 15 VDC supplies)
    - I/O address: 8-A HEX



- Example #6
  - Configuration:
    - Number of input channels: 8 differential
    - Input voltage range: 0-5V
    - I/O address: 3C-3E HEX
    - Interrupts: enabled



# ***Appendix***

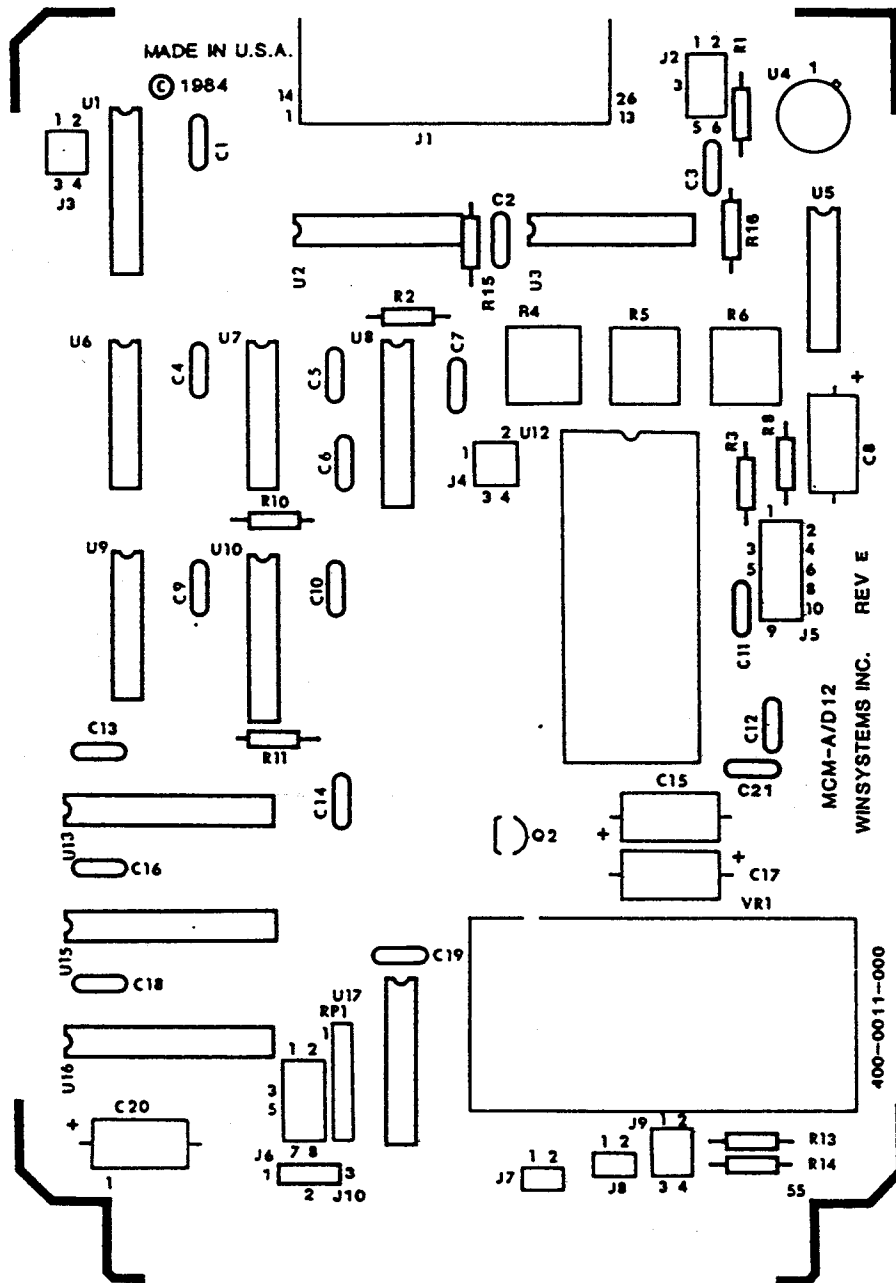
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Schematic Diagram  
LPM-A/D12 Parts List  
MCM-A/D12 Parts List  
Parts Placement Diagram  
Warranty and Repair Information





LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	MCM-A/D12	12-BIT A/D					1
2	0011-200-0000	ASSY MCM-A/D12 REV E	ASSY MCM-A/D12 REV D	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	03-01-91	ARLIN		Inv	1
3	>110-0004-001	CAP 500 PF MICA RAD CD15FD1501J0	C6	ARLIN		Inv	1
3	>110-0005-001	CAP 1K PF MICA RAD CD15FA102J03	C7	ARLIN		Inv	1
3	>110-0010-003	CAP .1 UF CER RAD SR215E104MAA	C1-C5,C9-C14,C16,C18,C19,C21	ARLIN		Inv	15
3	>110-0017-002	CAP 22 UF ALU ELEC AX TLB1C220M	C15,C17,C20	ARLIN		Inv	3
3	>113-0103-101	POT 10K RJ24-FW103	R5,R6	ARLIN		Inv	2
3	>114-0100-450	RESISTOR 10 OHM 1/4 5%	R13,R14	ARLIN		Inv	2
3	>114-0153-450	RESISTOR 15K 1/4 5%	R10	ARLIN		Inv	1
3	>114-0272-450	RESISTOR 2.7K 1/4 5%	R11	ARLIN		Inv	1
3	>115-0103-050	RM SIP 6P-5 RES 10K SRDSA-06P-C1	RP1	ARLIN		Inv	1
3	>125-0001-000	TRANSISTOR PN2222	Q2	ARLIN		Inv	1
3	>134-1004-410	RESISTOR 1.0M 1%	R3,R8	ARLIN		Inv	2
3	>134-1183-410	RESISTOR 118K 1%	R2	ARLIN		Inv	1
3	>200-0163-100	SOCKET 16 PIN ICO-163-S8A-T (220	U2,U3	ARLIN		Inv	2
3	>201-0026-121	HDR 26 POS RA IDH-26LP-SR3-TG/TR	J1	ARLIN		Inv	1
3	>201-0036-010	HDR 1X36 UN TSW-136-07-G-S	J7=1X2, J10=1X3	ARLIN		Inv	.138
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J2=2X3, J3,J4=2X2, J5=2X5,	ARLIN		Inv	.444
3	>999-9999-001	SPECIAL NOTES	J6=2X4 MADE FROM 2X36	ARLIN		Inv	1
3	>250-0320-200	SCKT STRIP 32 POS SS-132-G-2	U12	ARLIN		Inv	1
3	>340-0000-100	IC, 74LS00	U9	ARLIN		Inv	1
3	>340-0032-100	IC, 74LS32	U7	ARLIN		Inv	1
3	>340-0074-100	IC, 74LS74	U6	ARLIN		Inv	1
3	>340-0085-100	IC, 74LS85	U17	ARLIN		Inv	1
3	>340-0138-100	IC, 74LS138	U10	ARLIN		Inv	1
3	>340-0175-100	IC, 74LS175	U1	ARLIN		Inv	1
3	>340-0221-100	IC, 74LS221	U8	ARLIN		Inv	1
3	>340-0240-100	IC, 74LS240	U13,U15	ARLIN		Inv	2
3	>340-0245-100	IC, 74LS245	U16	ARLIN		Inv	1
3	>400-0011-000	PCB A/D 12 REV E (T)	PCB A/D 12 REV E (T)	ARLIN		Inv	1
3	>500-0001-000	EJECTOR SCANBE S208	STAMP (RED A/D12	ARLIN		Inv	1
3	>500-0002-000	ROLL PIN		ARLIN		Inv	1
3	>730-0011-000	IC, INA101AM	U4	ARLIN		Inv	1
3	>730-0025-000	IC, AD 585 AQ	U5	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	JUMPER WIRE J9=1-2,3-4,	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	MASK HOLES FOR R1,R15,R16	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	MASK HOLES FOR C8, VR1	ARLIN		Inv	1
2	0011-400-0000	SUB ASSY MCM-A/D12 REV E	SUB ASSY MCM-A/D12 REV D	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	03-01-91	ARLIN		Inv	1
3	>110-0015-004	CAP .001 POLY PRO AX 23PS210	C8	ARLIN		Inv	1
3	>201-0002-000	PLUG JUMPER 999-19-310-00	J5=1-2 5-6 9-10	ARLIN		Inv	7
3	>999-9999-001	SPECIAL NOTES	J3 1-2 3-4, J4=3-4	ARLIN		Inv	1
3	>730-0005-000	IC, DG508ACJ	U2,U3	ARLIN		Inv	2
3	>730-0014-000	IC, ADC80-12	U12	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	WIRE WRAP J2 1-3-4 2-6,	ARLIN		Inv	1



COMPONENT LAYOUT