OPERATIONS MANUAL
MCM-CTC

WinSystems, Inc. reserves the right to make changes in the circuitry and specifications at any time without notice.

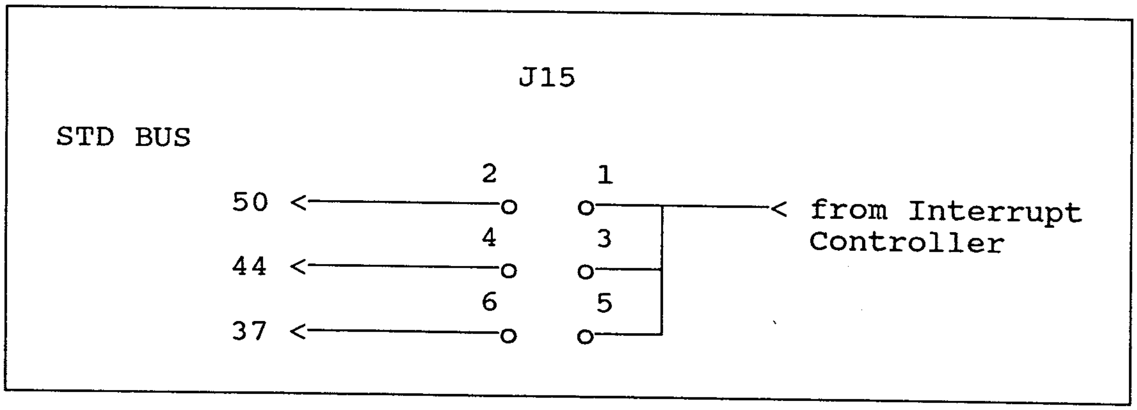
REVISION HISTORY
P/N 403-0069-000

ECO Number	Date Code	Rev Level
ORIGINATED	102487	A
91-04	060391	B
91-66	100991	B1

LPM/MCM-CTC ADDENDUM

The LPM/MCM-CTC has been modified in the following ways:

1. Jumper block J15 has been modified to allow STD BUS pin 37 to be used as an interrupt line on the backplane. See figure below.



2. A resistor R4 has been added as a user option for use with the on board 71059 interrupt controller when it is programmed in the slave mode. When the CTC is programmed for the slave interrupt mode, R4 should be installed with a value of 330 ohms.

3. These modifications effect revision B boards and higher.

TABLE OF CONTENTS

SECTION 1

MCM-CTC 9 Channel Counter/Timer

1.1 FEATURES

* Nine independent 16-bit Counter/Timers
* Uses 3 standard 8254 Programmable Interval Timers
* Six programmable counter modes per channel
* Handles inputs from DC to 8 MHz
* Binary or BCD counting
* Clock, Gate, and Out signals from 8 channels buffered and accessed via 2 connectors
* Channel 9 configurable as clock source for other channels
* Optional 8259A Interrupt controller
* Configurable Watchdog timer
* Single +5 volt supply
* STD Bus compatible

The MCM-CTC card is designed to solve the common timing problems in industrial systems design. Nine independent 16-bit channels are capable of frequency/event counting from DC to 8 MHz, pulse marker or square wave generation, time interval measurements, and one-shot simulation. Eight channels have a buffered Clock, Gate, and Output available at the top of the card. Jumpers header provide source selection and cascading to yield maximum configuration flexibility.

1.2 FUNCTIONAL CAPABILITY

Bus Interface - Full data, address, and control line buffering is provided to and from the STD Bus. It supports the STD-8Ø88 interrupt priority scheme either over the front or backplane. It can be operated with system clocks up to 8 MHz.

Addressing - The MCM-CTC is I/O mapped for either 8 or 1Ø-bit I/O addressing and is jumper configurable to start on any even 16 byte boundary. The card is accessed through Read and Write commands by the CPU. The three 8254 counter/timers require a total of 12 contiguous bytes starting at a base address of zero. Address lines A8 and A9 are decoded for the optional 1Ø-bit addressing mode. IOEXP* is decoded as active high, active low, or don't care and can be used to double the addressing range.

Counter/Timers - The MCM-CTC utilizes three 8254 programmable interval timers that can be individually configured to be real time clocks, event counters, digital one-shots, square wave generators, or programmable rate generators. Each 8254 contains three independent software programmable counter/timers yielding a total of nine 16-bit channels. The individual channels can be cascaded for longer count sequences.

The three internal 8254 counters are identical in operation. Each consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the Control Word Register. The status of the contents of each counter is available to the computer with a simple READ operation for event counting applications. Special logic is included so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

Watchdog Timer - The nineth channel can alternatively be used as a watchdog timer. This channel, programmed in the retriggerable one-shot mode, can have its output jumpered to the PBRESET* line of the STD Bus which will force a system reset in case of a software malfunction.

Time Base Clock - The nineth channel can also serve as a jumper selectable clock input to any of the other 8 channels for use in interval measurements. Either the System Clock or a onboard 2.4576 MHz crystal oscillator drives a dual divide by 2, 4, 8, or 16 prescaler that is input to Channel 9 and available to the other counters via the configuration header. The output of Channel 9's counter can be used to further scale the clock and its corresponding output is available to the other 8 channels.

Configuration Headers - Access to the Clock, Gate, Out and the boards Time Base Clock is provided for all channels. A select header is provided to permit jumpering clock inputs from the I/O Connectors, Channel 9, or the System Clock.

Connector Configuration - The MCM-CTC has two, 26-pin connectors that permit access to the Clock, Gate and Out signals for each channel. The connectors are grouped with 4 channels per connector. All the signals are fully buffered on and off the board. Each signal line is paired with a ground line to prevent adjacent noise and crosstalk. All input lines have Schmitt trigger circuits to prevent oscillation from signals with slow rise and fall times.

J1 and J2 Connector Pinout

J1 Pin	Channel Ø - 3 Signal	J2 Pin	Channels 4 - 7 Signal
1	Gate Ø*	1	Gate 4*
3	Clock Ø*	3	Clock 4*
5	Out Ø*	5	Out 4*
7	Gate 1*	7	Gate 5*
9	Clock 1*	9	Clock 5*
11	Out 1*	11	Out 5*
13	Gate 2*	13	Gate 6*
15	Clock 2*	15	Clock 6*
17	Out 2*	17	Out 6*
19	Gate 3*	19	Gate 7*
21	Clock 3*	21	Clock 7*
23	Out 3*	23	Out 7*
25	+5 volts	25	+5 volts

* = Low-level active logic
Even pins (2, 4, 6, etc.) are ground

Interrupts - The MCM-CTC will generate STD-8Ø88 compatible interrupts when an optional 8259A PIC is installed (MCM-CTC-1). The PIC generates a unique, vectored interrupt for each of the 8 CTC channels.

The PIC will operate in the slave mode and support cascade interrupts over the STD Bus address lines A8 - A1Ø. Interrupt requests can be generated either over the front plane or by INTRQ* or CNTRL* on the backplane. Selection is jumper selectable.

1.3 SPECIFICATIONS

Electrical

System Clock:	Up to 8 MHz
Mapping:	Occupies 12 sequential I/O ports; may be remapped on any even 16 port boundary. IOEXP: Jumper configurable as active high, active low, or don't care
Interface:	Inputs - All inputs are 74LS/TTL levels Output - All outputs are 74LS/TTL levels
Power:	+5V +/- 1Ø% at 25Ø mA typ.

Mechanical

Dimensions:	Meets all STD Bus Specifications, 4.5 x 6.5 inches
PC Board:	FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

Channel:	Two, 26-pin dual on Ø.1ØØ grid
Interrupt:	1Ø-pin dual on Ø.1ØØ inch grid
Jumpers:	Ø.Ø25 inch square posts

Environmental

Operating Temperature: Ø°C to +65°C
Non-condensing relative humidity: 5% to 95%

1.4 ORDERING INFORMATION

MCM-CTC-Ø	Nine channel 16-bit counter/timer card
MCM-CTC-1	Nine channel 16-bit counter/timer card with 8259 Programmable Interrupt Controller

SECTION 2

USER OPTIONS

2.1 I/O ADDRESS DECODER

2.1.1 The MCM-CTC has a jumper selectable I/O address decoder so that more than one MCM-CTC board can be used in a system. The MCM-CTC can decode up to ten address bits A0-A9 and can be positioned on any 32 I/O port boundary, i.e., 0-13, 20-33, etc. The I/O address for the MCM-CTC is controlled by jumper blocks J11 and J12 and are shown in Figure 2-1. If J11 is left open, and pins 1,2,3,4,5, and 6 are left open on J12, then the MCM-CTC will only decode the lower eight bits of the I/O address A0-A7, and the /IOEXP signal will be ignored by the I/O decoder.

NOTE: The 10 bit addressing mode should only be used with processor boards that use the 80XXX, V20-V60, HD64180, 68XXX, or any processor that generates a 10 bit or higher I/O address. The 8 bit mode MUST be used with Z80 or 8085 processor boards.

FIGURE 2-1
I/O ADDRESS DECODER JUMPER BLOCKS J11 AND J12

```
                 J12

          1   3   5   7   9  11
          o   o   o   o   o   o  "1" = OPEN

          o   o   o   o   o   o   "0" = JUMPER
          2   4   6   8  10  12

     /IOEXP  A9  A8  A7  A6  A5
```

NOTE: For 8 bit addressing, pins 3,4,5, and 6 of J12 should be left open. J12 pins 1-2 are used to set /IOEXP high or low.

```
         J11

       1   3   5
       o   o   o

       o   o   o
       2   4   6
  /IOEXP  A9  A8
```

Jumper block J11 is used for enabling\disabling the 10 bit addressing mode and /IOEXP. To enable 10 bit addressing connect

J11 3-4, and 5-6. The corresponding bits can then be used on J12 to select the I/O address and /IOEXP for the MCM-CTC. /IOEXP can be enabled or disabled by J11. To enable /IOEXP, connect J11 1-2.

2.2. 82C54/71054 COUNTER/TIMERS

2.2.1. The MCM-CTC was designed using the 82C54/71054 counter/timer chip. Before the 82C54/71054 can be used it first must be initialized by outputting several command/control words that sets up the mode of operation. The 82C54/71054 datasheet is included in the APPENDIX for reference and the first time user of the 82C54/71054 is encouraged to read over the data sheet before trying to use the MCM-CTC.

2.2.2. Each 82C54/71054 uses four I/O ports for accessing each of the three channels and the one channel for command/control. Table 2-1 shows the I/O port assignment of the three 82C54/71054's and the 82C59A/71059 interrupt controller.

TABLE 2-1
I/O PORT ASSIGNMENT FOR 82C54/71054's AND 82C59A/71059

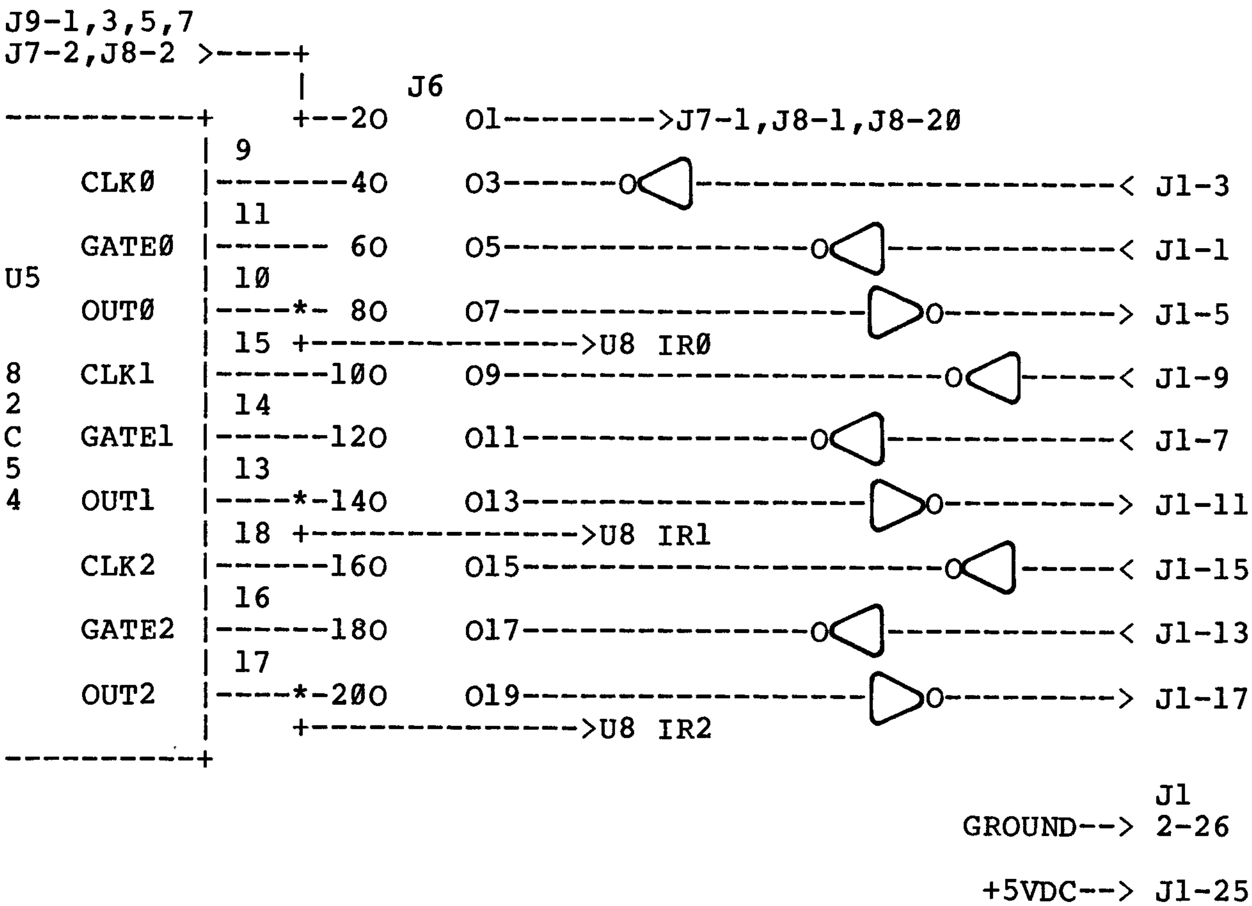
DEVICE		I/O PORT	FUNCTION
(PIT) 82C54/71054	U5	aaaaa00000	COUNTER 0
		aaaaa00001	COUNTER 1
		aaaaa00010	COUNTER 2
		aaaaa00011	CONTROL
(PIT) 82C54/71054	U6	aaaaa00100	COUNTER 0
		aaaaa00101	COUNTER 1
		aaaaa00110	COUNTER 2
		aaaaa00111	CONTROL
(PIT) 82C54/71054	U7	aaaaa01000	COUNTER 0
		aaaaa01001	COUNTER 1
		aaaaa01010	COUNTER 2
		aaaaa01011	CONTROL
(PIC) 82C59A/71059	U8	aaaaa01100	COMMAND/CONTROL
		aaaaa01101	COMMAND/CONTROL
		aaaaa01110	REDUNDANT
		aaaaa01111	"
WATCHDOG TIMER CONTROL		aaaaa10000	WATCHDOG ENABLE/TRIGGER
		aaaaa10001	REDUNDANT
		aaaaa10010	"
		aaaaa10011	"

NOTE: (1) aaaaa REPRESENTS THE PROGRAMMABLE I/O ADDRESS THAT IS JUMPER PROGRAMMABLE BY THE USER FOR 8 OR 10 BITS.

2.3. J1/J2 CONNECTOR PIN-OUTS

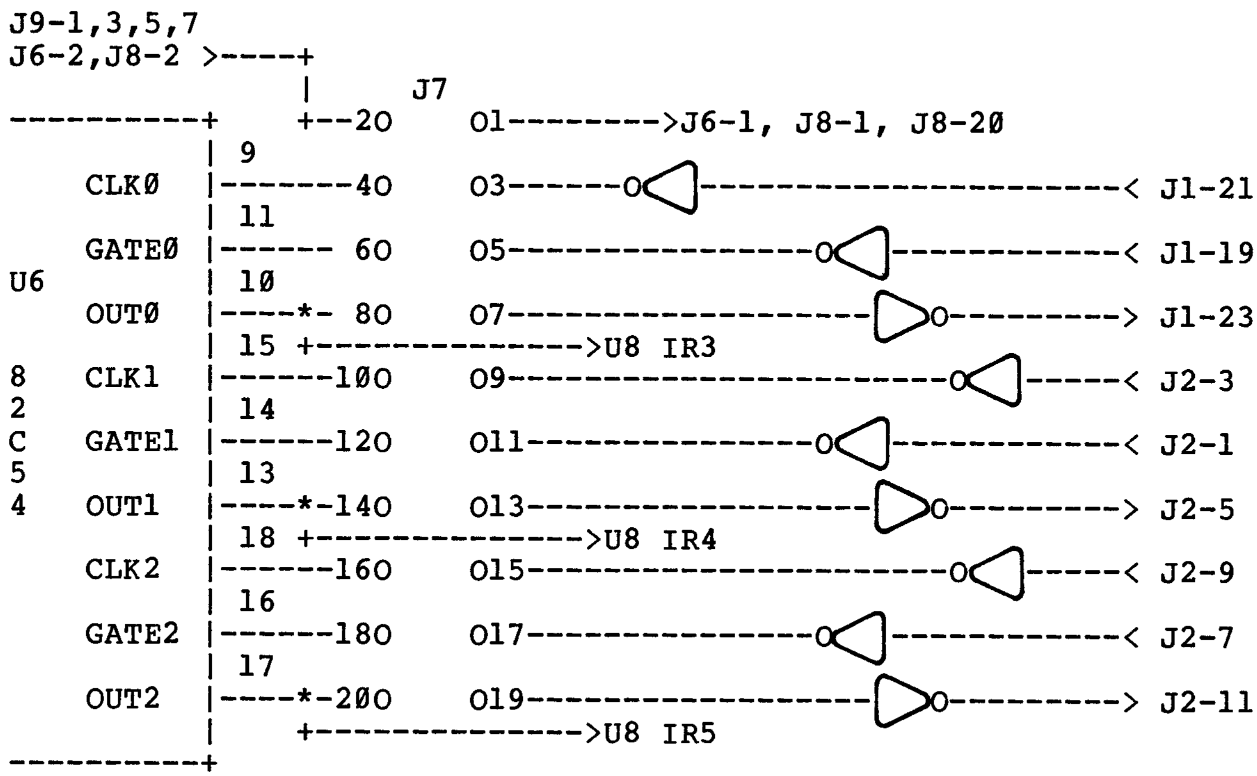
2.3.1. All of the 82C54/71054 I/O functions are brought out to the connectors J1 and J2 through several jumper blocks that are labeled J6-J8. These jumper blocks allow the user to chain channels together for longer time delays or other special applications. Figures 2-2a,b,c show the relationship of the jumper blocks J6-J8 and their associated pin-outs to J1 and J2.

FIGURE 2-2a
J6-J8, J1 AND J2 PIN-OUTS



NOTE: ALL INPUTS ON THE 82C54/71054 AND BUFFER IC'S HAVE A 10K OHM PULL-UP RESISTOR.

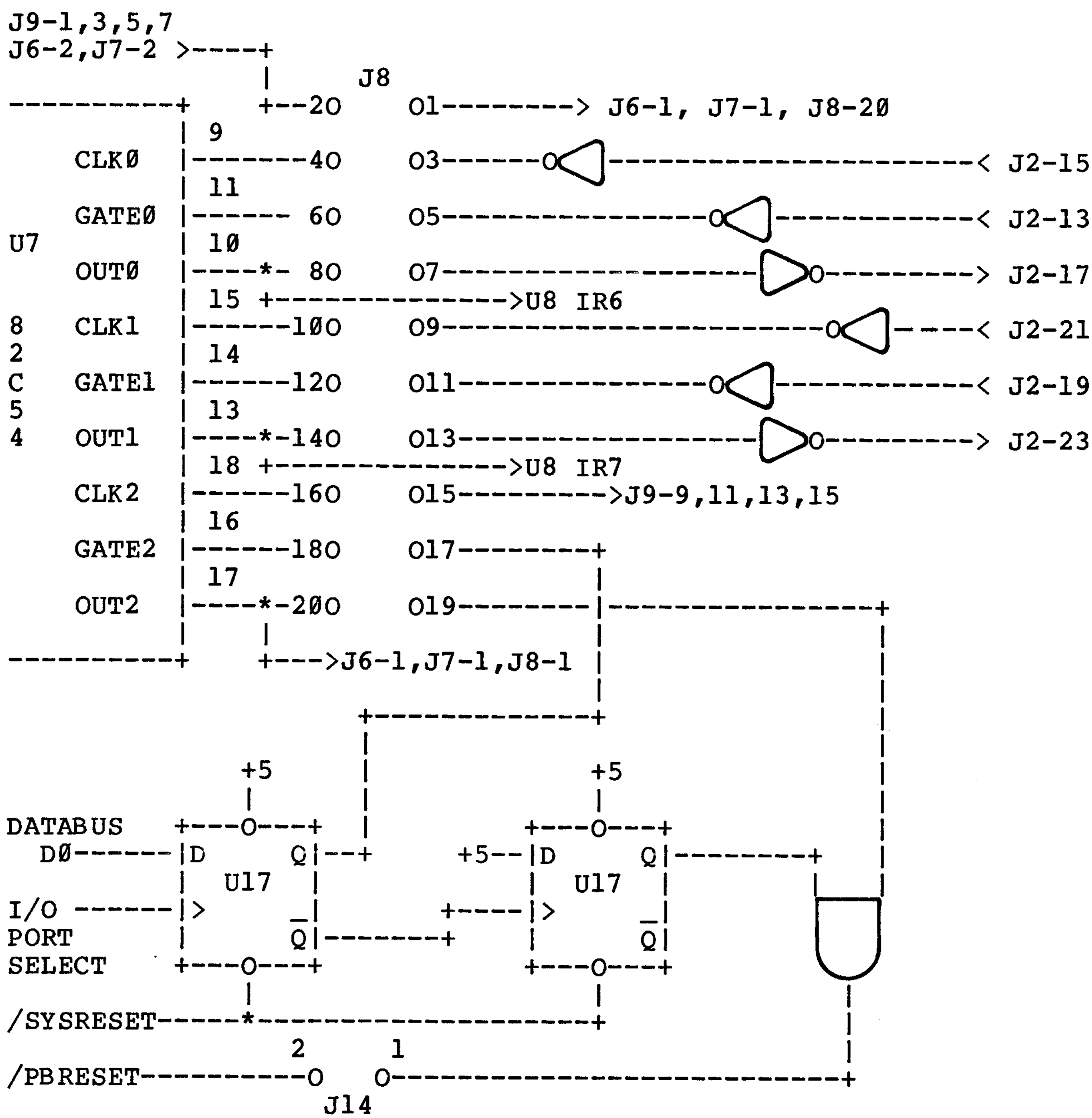
FIGURE 2-2b
J6-J8, J1 AND J2 PIN-OUTS



J2
GROUND--> 2-26

+5VDC--> J1-25

FIGURE 2-2c
J6-J8, J1 AND J2 PIN-OUTS



WATCHDOG TIMER

2.4 INTERRUPTS

2.4.1. The MCM-CTC can be jumpered to generate an interrupt from an 82C59A/71Ø59 interrupt controller onto the STD BUS or be connected to connector J3 to take the interrupt request "over the top" of the board to the CPU board. J15 will allow the MCM-CTC to generate an active low interrupt to one of two pins on the STD BUS. They are:

pin 44 (/INTRQ)
pin 5Ø (Alternate interrupt line)

NOTE: 1. Pin 5Ø is provided to allow additional interrupt sources on the STD BUS.

2. The 82C59A/71Ø59 interrupt controller must programmed for the desired interrupts.

2.4.2. Figure 2-3 shows the interrupt select jumper J15.

FIGURE 2-3
J15 INTERRUPT SELECT

J15

2O	O1
4O	O3

TO ENABLE THE CTC INTERRUPT TO STD BUS PIN #44 (INTRQ)

CONNECT J15 3-4

TO ENABLE THE CTC INTERRUPT TO STD BUS PIN #5Ø

CONNECT J15 1-2

2.4.3. The 82C59A/71Ø59 interrupt controller on the MCM-CTC can be used in several ways. They are:

(1) As a "Master Interrupt Controller" when used with 8Ø85 or other processors that DO NOT have another 82C59A/71Ø59 interrupt controller.

(2) As a "Slave Interrupt Controller" when used with another 82C59A/71Ø59 that is programmed as the Master Interrupt Controller. This application is typically used with the 8ØXXX style of CPU boards, and should meet the STDMG 8Ø88 specification for handling Cascade Interrupts.

2.4.4. The 82C59A/71Ø59 interrupt controller on the MCM-CTC is typically used with 8ØXXX processor boards and is programmed to perform in the Cascade interrupt mode. Before attempting the programming of the 82C59A/71059, the first time user of the 82C59A/71059 is directed to the INTEL applications note AP-59 that goes into great detail in describing the operation of the 82C59A/71059. The datasheet for the 82C59A/71059 is included in the APPENDIX.

2.4.5. The interrupt request inputs (IR0-IR7), cascade inputs, and the interrupt output for the 82C59A/71059 interrupt controller is shown in Figure 2-4.

FIGURE 2-4
82C59A/71059 INTERRUPT CONTROLLER

```
          +----------+
          |      IR0|-----U5 OUT0
          |         |
          |      IR1|-----U5 OUT1
          |         |
          |U8    IR2|-----U5 OUT2
          |         |
          |8     IR3|-----U6 OUT0
          |2        |                                J4
          |C     IR4|-----U6 OUT1                   2     1
          |5        |                            +---O  O--->J3-2
          |9     IR5|-----U6 OUT2                |  4     3
          |A        |                            *---O  O--->J3-4
     J13  |      IR6|-----U7 OUT0                |  6     5
          |         |                            *---O  O--->J3-6
   2    1 |      IR7|-----U7 OUT1                |  8     7
A8--O  O--|CAS0     |                    J5      *---O  O--->J3-8
   4    3 |         |                  2     1   | 10     9
A9--O  O--|CAS1     |  +----------------O   O----*---O  O--->J3-10
   6    5 |         |  |               4     3   |
A10-O  O--|CAS2  INT|--*-------|>o------O   O----+
          |         |
          +----------+

                                                  GROUND---J3
                                                           1-9
```

NOTES: (1) THE 82C59A/71059 MUST BE PROGRAMMED FOR THE "BUFFERED SLAVE" OR "BUFFERED MASTER" MODE.

(2) WHEN USING THE MCM-CTC IN THE "SLAVE MODE" CONNECT J13 1-2, 3-4, 5-6.

(3) WHEN USING THE MCM-CTC IN THE "MASTER MODE" LEAVE J13 1-2, 3-4, 5-6 OPEN.

(4) J3 2-10 IS FOR "OVER THE TOP" INTERRUPTS TO THE CPU CARD. FOR "ACTIVE HIGH" INTERRUPTS CONNECT J5 1-2, FOR "ACTIVE LOW" INTERRUPTS CONNECT J5 3-4.

(5) J4 IS USED TO SELECT THE APPROPRIATE "OVER THE TOP" INTERRUPT LEVEL ON THE CPU CARD.

2.5. TIME BASE CLOCK GENERATOR

2.5.1. The MCM-CTC has a separate time base clock generator that can be driven by the STD BUS /CLOCK or from an on-board 4.9152 MHz oscillator. The output from the time base generator is /2, /4, /8, /16, /32, /64, /128 or /256. These outputs are brought out to J9, and can be then jumpered to the inputs of the 82C54/71054 counter/timers through jumper blocks J6, J7, and J8. See Figure 2-5. Jumper block J10 is used to select the clock source for the time base.

```
                    +---------+       J9
                    |         |  2     1
                    |      /2 |----O   O----*-------> J6-2
                    |         |  4     3    |         J7-2
+-----------+       |      /4 |----O   O----*         J8-2
|4.1952 MHz |       |         |  6     5    |
|OSCILLATOR |       |      /8 |----O   O----*
|           |       | U10     |  8     7    |
+-----------+       |     /16 |----O   O----+
/    J10            |         | 10     9
| 2     1           |     /32 |----O   O----*-------> J8-15
+--O   O---*--------|>        | 12    11    |
  4     3  |        |     /64 |----O   O----*
   O   O---+        |         | 14    13    |
   |                |    /128 |----O   O----*
   |                |         | 16    15    |
+-------+           |    /256 |----O   O----+
|STD BUS|           |         |
|/CLOCK |           +---------+
+-------+
```

2.6. WATCHDOG TIMER OPERATION

2.6.1. The MCM-CTC has special circuitry on board, when used with the output of channel 2 of the 82C54/71054 U7, can be used as a Watchdog Timer. To use the watchdog timer, do the following:

(1) CONNECT: J8 15-16, 17-18, 19-20; J14 1-2.

(2) SELECT AN OUTPUT FROM THE TIME BASE OUTPUT JUMPER BLOCK J9.

(3) CHANNEL 2 OF THE 82C54/71054 MUST BE PROGRAMMED FOR THE RETRIGGERABLE ONE-SHOT MODE.

(4) THE WATCHDOG TIMER IS ENABLED AND TRIGGERED BY FIRST SETTING THE LSB OF I/O PORT aaaaa10000 HIGH TO TRIGGER THE 82C54/71054. THE LSB OF I/O PORT aaaaa10000 SHOULD BE SET LOW ONLY AFTER 2 INPUT CLOCK PERIODS HAVE ELAPSED.(THE CLOCK PERIOD IS THE INPUT TO CHANNEL 2 OF U7).

(5) THE LSB OF I/O PORT WILL HAVE TO BE TOGGLED (LOW TO HIGH TO LOW) BEFORE THE WATCHDOG TIMER PERIOD ELAPSES.

(6) IF THE WATCHDOG TIMER TIMES OUT, THE PROCESSOR WILL BE RESET, AND THE WATCHDOG TIMER WILL BE DISABLED.

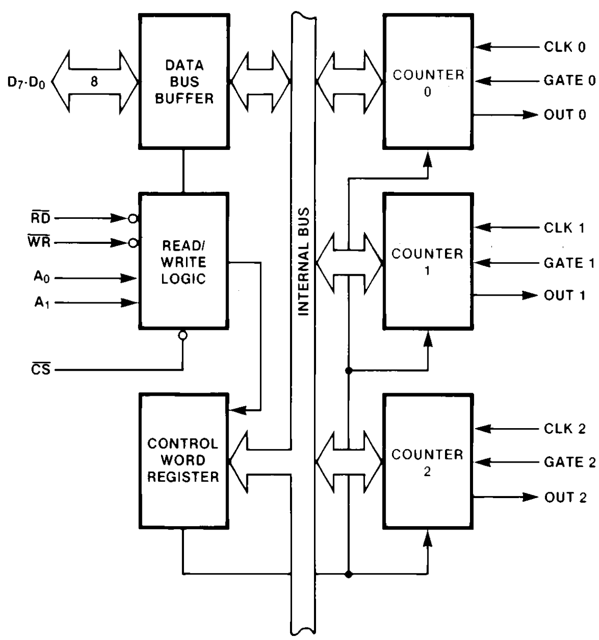
APPENDIX

8254
PROGRAMMABLE INTERVAL TIMER

- **Compatible with All Intel and Most Other Microprocessors**
- **Handles Inputs from DC to 10 MHz**
  — 8 MHz 8254
  — 10 MHz 8254-2
- **Status Read-Back Command**
- **Six Programmable Counter Modes**
- **Three Independent 16-Bit Counters**
- **Binary or BCD Counting**
- **Single +5V Supply**
- **Available in EXPRESS**
  — Standard Temperature Range

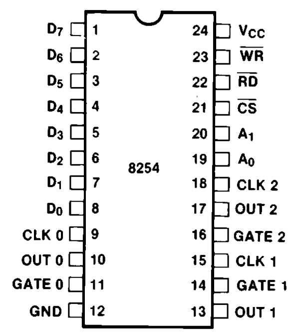
The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.



231164–1

Figure 1. 8254 Block Diagram



231164–2

Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
D_7-D_0	1–8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** +5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20–19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus. **A_1 / A_0 / Selects** 0 / 0 / Counter 0 0 / 1 / Counter 1 1 / 0 / Counter 2 1 / 1 / Control Word Register
CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

FUNCTIONAL DESCRIPTION

General

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus (see Figure 3).

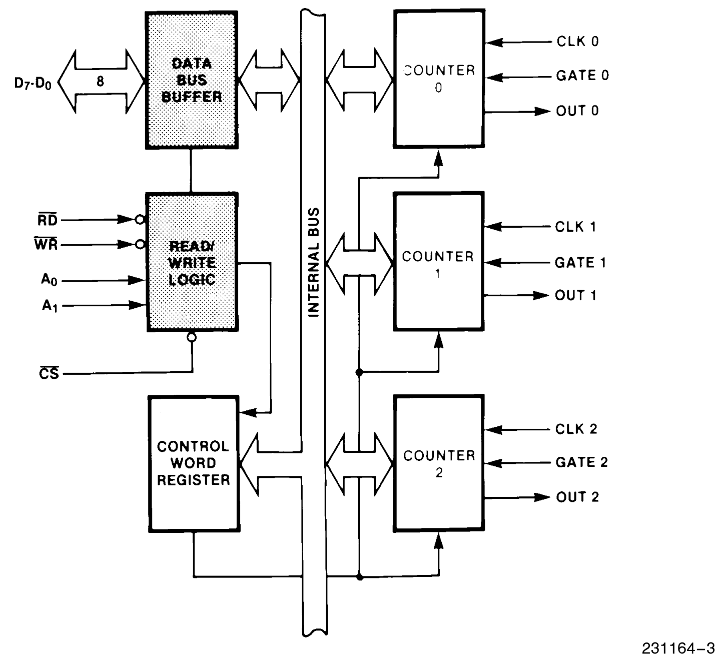


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

READ/WRITE LOGIC

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 8254. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 8254 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 8254 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 8254 has been selected by holding $\overline{CS}$ low.

CONTROL WORD REGISTER

The Control Word Register (see Figure 4) is selected by the Read/Write Logic when $A_1,A_0 = 11$. If the CPU then does a write operation to the 8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

COUNTER 0, COUNTER 1, COUNTER 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in Figure 5, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte"

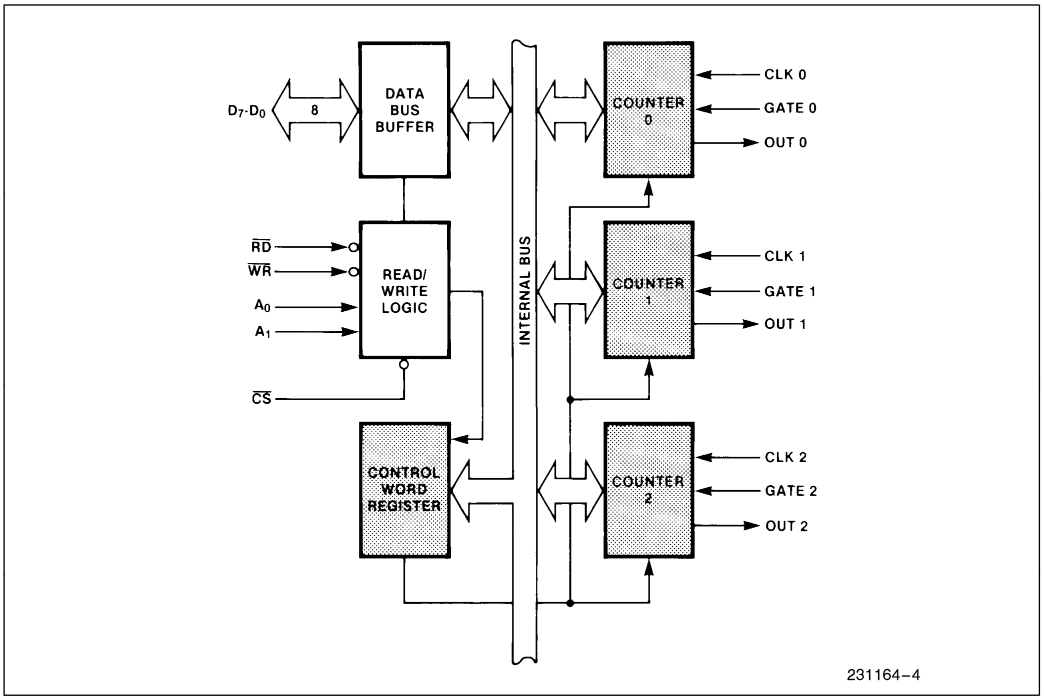


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

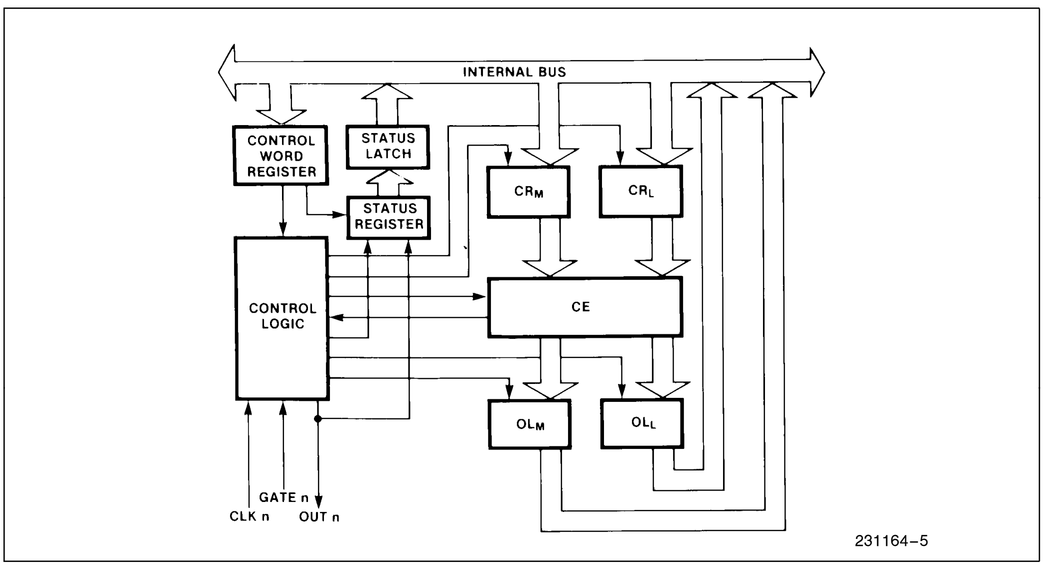


Figure 5. Internal Block Diagram of a Counter

respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 8254, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

8254 SYSTEM INTERFACE

The 8254 is a component of the Intel Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the system's software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0,A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

OPERATIONAL DESCRIPTION

General

After power-up, the state of the 8254 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 8254

Counters are programmed by writing a Control Word and then an initial count.

The Control Words are written into the Control Word Register, which is selected when A_1,A_0 = 11. The Control Word itself specifies which Counter is being programmed.

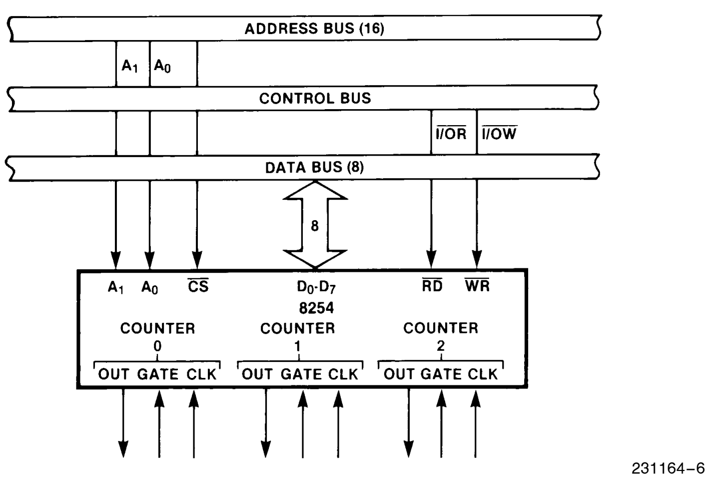


Figure 6. 8254 System Interface

Control Word Format

$A_1,A_0 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1,A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the 8254 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.
2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1,A_0 inputs), and each Control Word specifies the Counter it applies to (SC0,SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions in Figure 7 is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

	A_1	A_0
Control Word—Counter 0	1	1
LSB of count—Counter 0	0	0
MSB of count—Counter 0	0	0
Control Word—Counter 1	1	1
LSB of count—Counter 1	0	1
MSB of count—Counter 1	0	1
Control Word—Counter 2	1	1
LSB of count—Counter 2	1	0
MSB of count—Counter 2	1	0

	A_1	A_0
Control Word—Counter 2	1	1
Control Word—Counter 1	1	1
Control Word—Counter 0	1	1
LSB of count—Counter 2	1	0
MSB of count—Counter 2	1	0
LSB of count—Counter 1	0	1
MSB of count—Counter 1	0	1
LSB of count—Counter 0	0	0
MSB of count—Counter 0	0	0

	A_1	A_0
Control Word—Counter 0	1	1
Control Word—Counter 1	1	1
Control Word—Counter 2	1	1
LSB of count—Counter 2	1	0
LSB of count—Counter 1	0	1
LSB of count—Counter 0	0	0
MSB of count—Counter 0	0	0
MSB of count—Counter 1	0	1
MSB of count—Counter 2	1	0

	A_1	A_0
Control Word—Counter 1	1	1
Control Word—Counter 0	1	1
LSB of count—Counter 1	0	1
Control Word—Counter 2	1	1
LSB of count—Counter 0	0	0
MSB of count—Counter 1	0	1
LSB of count—Counter 2	1	0
MSB of count—Counter 0	0	0
MSB of count—Counter 2	1	0

NOTE:
In all four examples, all Counters are programmed to read/write two-byte counts. These are only four of many possible programming sequences.

Figure 8. A Few Possible Programming Sequences

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 8254.

There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command. Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

COUNTER LATCH COMMAND

The second method uses the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when $A_1,A_0 = 11$. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

$A_1,A_0 = 11$; $CS = 0$; $RD = 1$; $WR = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1,SC0—specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4—00 designates Counter Latch Command

X—don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 9. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 8254 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1) Read least significant byte.
2) Write new least significant byte.
3) Read most significant byte.
4) Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

READ-BACK COMMAND

The third method uses the Read-Back Command. This command allows the user to check the count value, programmed Mode, and current states of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{\text{COUNT}}$	$\overline{\text{STATUS}}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counters(s)
D_3: 1 = Select Counter 2
D_2: 1 = Select Counter 1
D_1: 1 = Select Counter 0
D_0: Reserved for future expansion; Must be 0

Figure 10. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the $\overline{\text{COUNT}}$ bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). The counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{\text{STATUS}}$ bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 11. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null Count	RW1	RW0	M2	M1	M0	BCD

D_7 1 = OUT Pin is 1
0 = OUT Pin is 0

D_6 1 = Null Count
0 = Count available for reading

D_5–D_0 Counter programmed mode (see Figure 7)

Figure 11. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.

This Action	Causes
A. Write to the control word register;(1)	Null Count = 1
B. Write to the count register (CR);(2)	Null Count = 1
C. New Count is loaded into CE (CR → CE);	Null Count = 0

NOTE:
1. Only the counter specified by the control word will have its Null Count set to 1. Null count bits of other counters are unaffected.
2. If the counter is programmed for two-byte counts (least significant byte then most significant byte) Null Count goes to 1 when the second byte is written.

Figure 12. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both $\overline{COUNT}$ and $\overline{STATUS}$ bits D5,D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Command D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description	Result
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

Mode Definitions

The following are defined for use in describing the operation of the 8254.

CLK Pulse: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

Trigger: a rising edge of a Counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

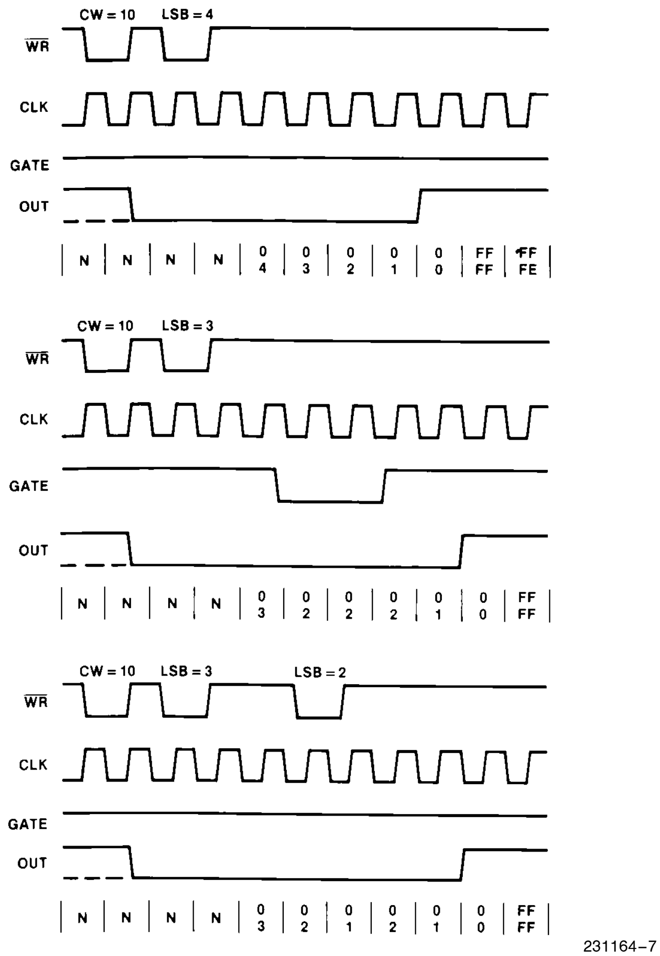
GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the



NOTE:
The following conventions apply to all mode timing diagrams:
1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10 HEX is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Figure 15. Mode 0

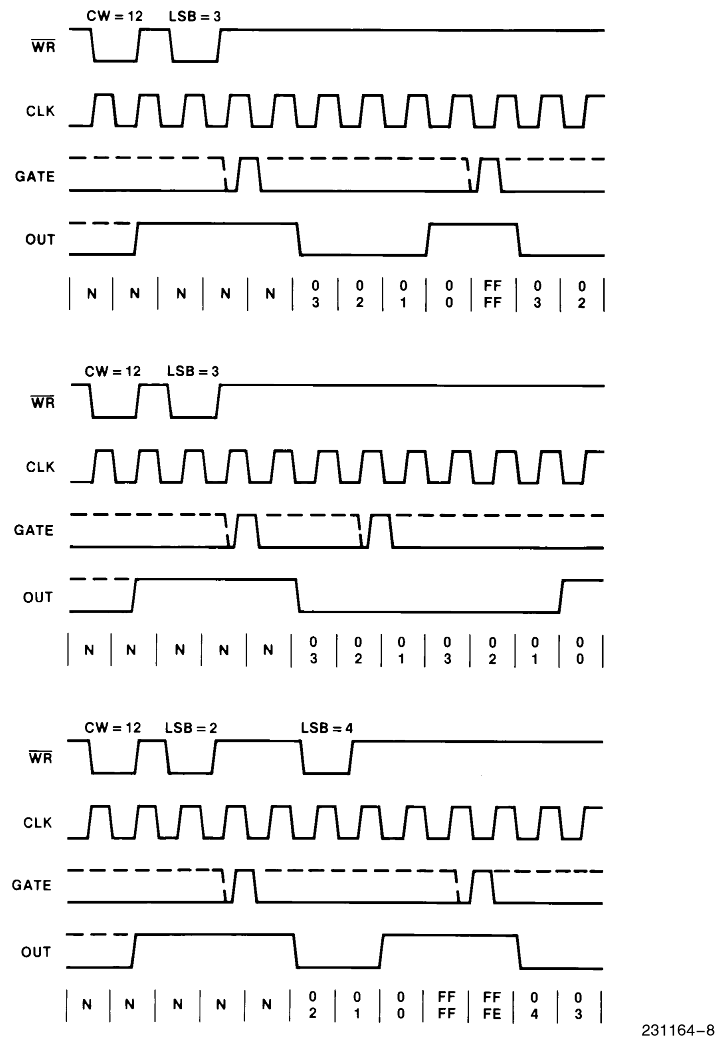


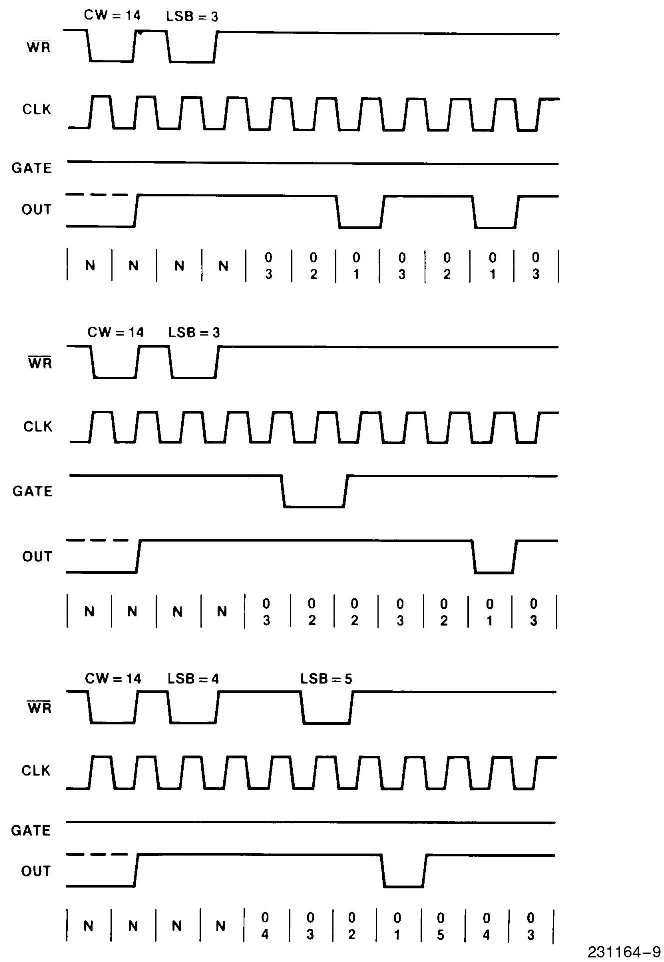
Figure 16. Mode 1

initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the



NOTE:
A GATE transition should not occur one clock prior to terminal count.

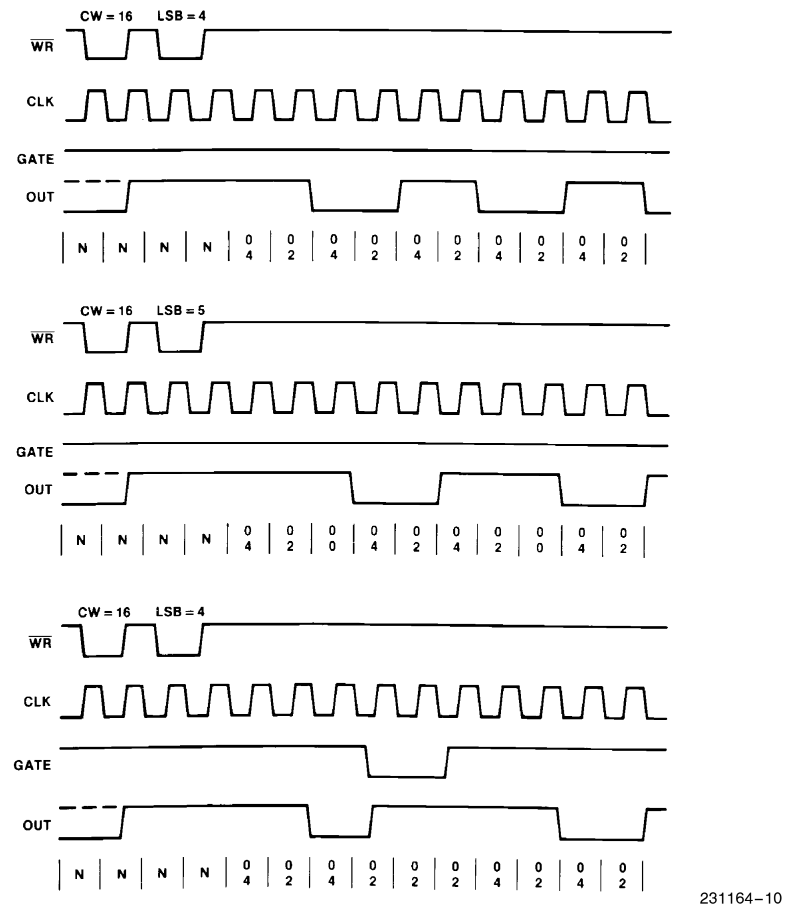
Figure 17. Mode 2

new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse *after* the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N − 1)/2 counts.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 18. Mode 3

MODE 4: SOFTWARE TRIGGERED STROBE

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

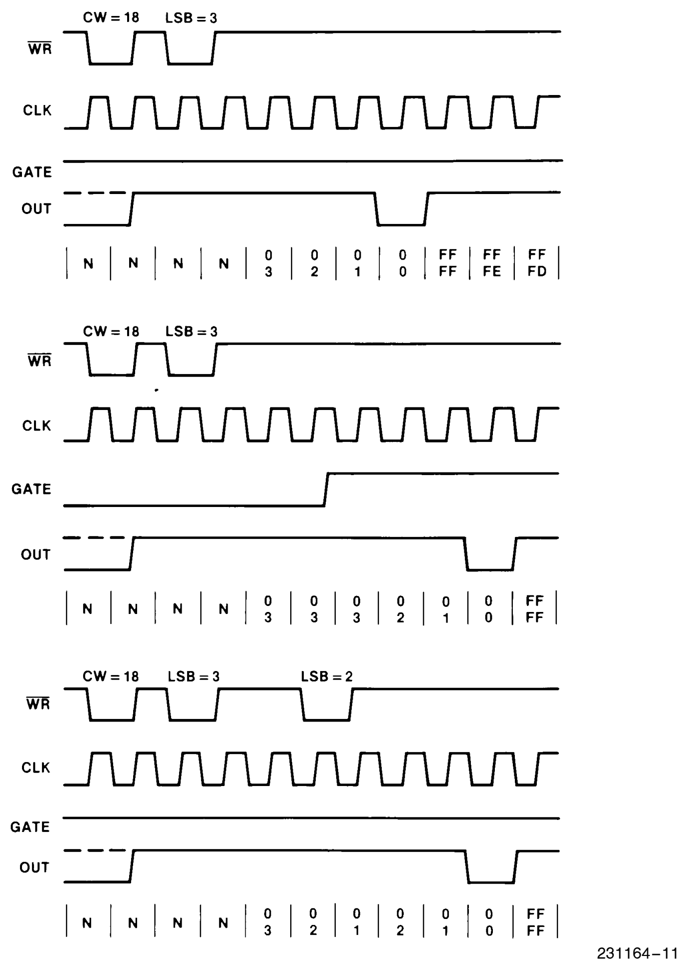


Figure 19. Mode 4

MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

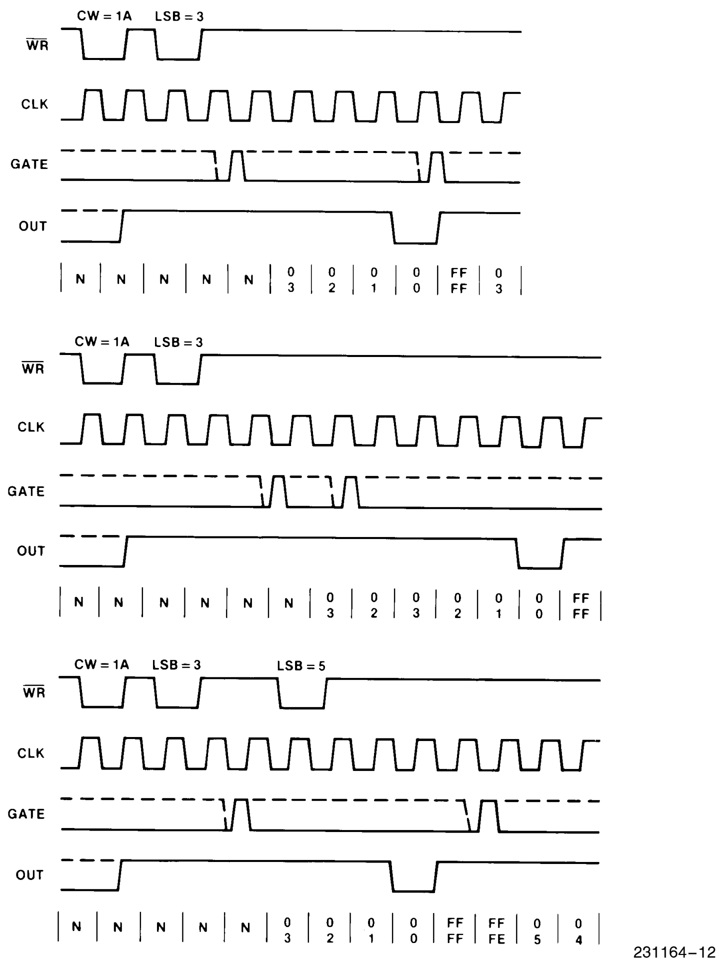


Figure 20. Mode 5

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	——	Enables Counting
1	——	1) Initiates Counting 2) Resets Output after Next Clock	——
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	——	Enables Counting
5	——	Initiates Counting	——

Figure 21. Gate Pin Operations Summary

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Figure 22. Minimum and Maximum Initial Counts

Operation Common to All Modes

PROGRAMMING

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs—a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

COUNTER

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter ‘‘wraps around’’ to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ......0°C to 70°C

Storage Temperature .... −65°C to +150°C

Voltage on Any Pin with
Respect to Ground.............. −0.5V to +7V

Power Dissipation 1W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0.45V
I_{CC}	V_{CC} Supply Current		170	mA	
C_{IN}	Input Capacitance		10	pF	f_c = 1 MHz
$C_{I/0}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}(4)

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Bus Parameters(1)

READ CYCLE

Symbol	Parameter	8254		8254-2		Unit
		Min	Max	Min	Max	
t_{AR}	Address Stable Before $\overline{RD}$ ↓	45		30		ns
t_{SR}	$\overline{CS}$ Stable Before $\overline{RD}$ ↓	0		0		ns
t_{RA}	Address Hold Time After $\overline{RD}$ ↑	0		0		ns
t_{RR}	$\overline{RD}$ Pulse Width	150		95		ns
t_{RD}	Data Delay from $\overline{RD}$ ↓		120		85	ns
t_{AD}	Data Delay from Address		220		185	ns
t_{DF}	$\overline{RD}$ ↑ to Data Floating	5	90	5	65	ns
t_{RV}	Command Recovery Time	200		165		ns

NOTE:
1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, GND = 0V (Continued)

WRITE CYCLE

Symbol	Parameter	8254		8254-2		Unit
		Min	Max	Min	Max	
t_{AW}	Address Stable Before $\overline{WR}$ ↓	0		0		ns
t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}$ ↓	0		0		ns
t_{WA}	Address Hold Time After $\overline{WR}$ ↓	0		0		ns
t_{WW}	$\overline{WR}$ Pulse Width	150		95		ns
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑	120		95		ns
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	0		0		ns
t_{RV}	Command Recovery Time	200		165		ns

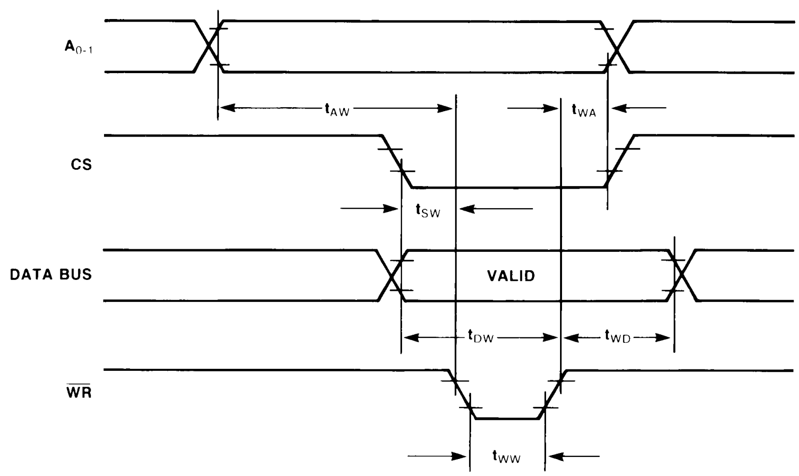
CLOCK AND GATE

Symbol	Parameter	8254		8254-2		Unit
		Min	Max	Min	Max	
t_{CLK}	Clock Period	125	DC	100	DC	ns
t_{PWH}	High Pulse Width	60(3)		30(3)		ns
t_{PWL}	Low Pulse Width	60(3)		50(3)		ns
t_R	Clock Rise Time		25		25	ns
t_F	Clock Fall Time		25		25	ns
t_{GW}	Gate Width High	50		50		ns
t_{GL}	Gate Width Low	50		50		ns
t_{GS}	Gate Setup Time to CLK ↑	50		40		ns
t_{GH}	Gate Setup Time After CLK ↑	50(2)		50(2)		ns
t_{OD}	Output Delay from CLK ↓		150		100	ns
t_{ODG}	Output Delay from Gate ↓		120		100	ns
t_{WC}	CLK Delay for Loading ↓	0	55	0	55	ns
t_{WG}	Gate Delay for Sampling	−5	50	−5	40	ns
t_{WO}	OUT Delay from Mode Write		260		240	ns
t_{CL}	CLK Set Up for Count Latch	−40	45	−40	40	ns

NOTES:
2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 8254-2) of the rising clock edge may not be detected.
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
4. Sampled, not 100% tested. T_A = 25°C.
5. If CLK present at TWC min then Count equals N+2 CLK pulses, TWC max equals Count N+1 CLK pulse. TWC min to TWC max, count will be either N+1 or N+2 CLK pulses.
6. In Modes 1 and 5, if GATE is present when writing a new Count value, at TWG min Counter will not be triggered, at TWG max Counter will be triggered.
7. If CLK present when writing a Counter Latch or ReadBack Command, at TCL min CLK will be reflected in count value latched, at TCL max CLK will not be reflected in the count value latched.

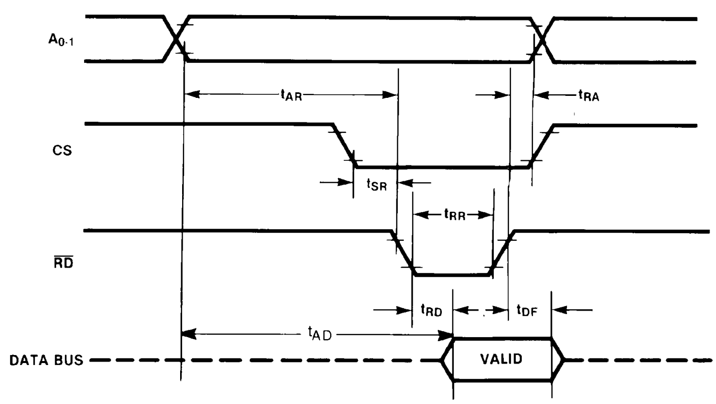
WAVEFORMS

WRITE



231164–13

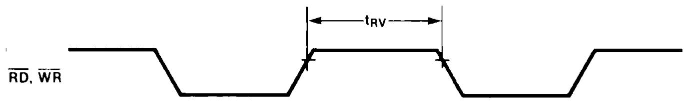
READ



231164–14

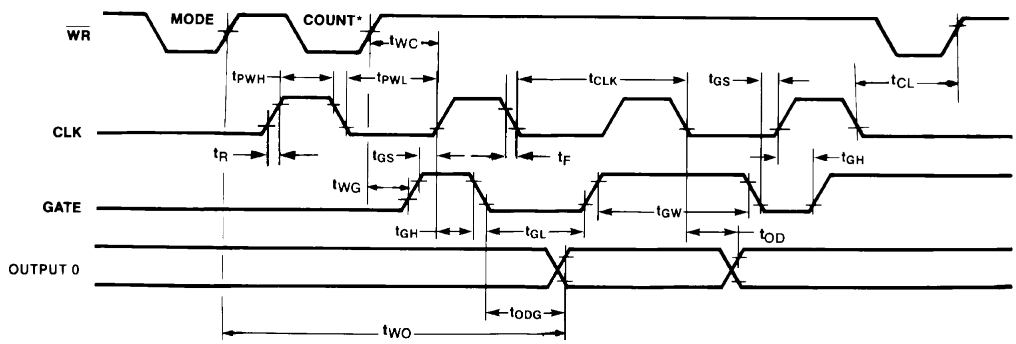
WAVEFORMS (Continued)

RECOVERY



231164–15

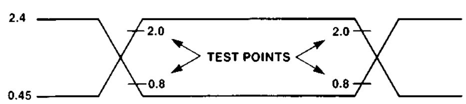
CLOCK AND GATE



231164–16

*Last byte of count being written.

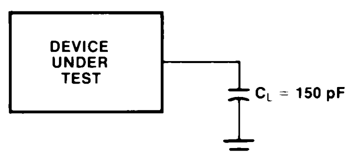
A.C. TESTING INPUT, OUTPUT WAVEFORM



231164–17

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



231164–18

C_L = 150 pF
C_L Includes Jig Capacitance

REVISION SUMMARY

The following list represents the key differences between Rev. 004 and Rev. 005 of the 8254 Data Sheet.

1. References to and specifications for the 5 MHz 8254-5 are removed. Only the 8 MHz 8254 and the 10 MHz 8254-2 remain in production.

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6 APPENDIX D

8259A Datasheet Reprint

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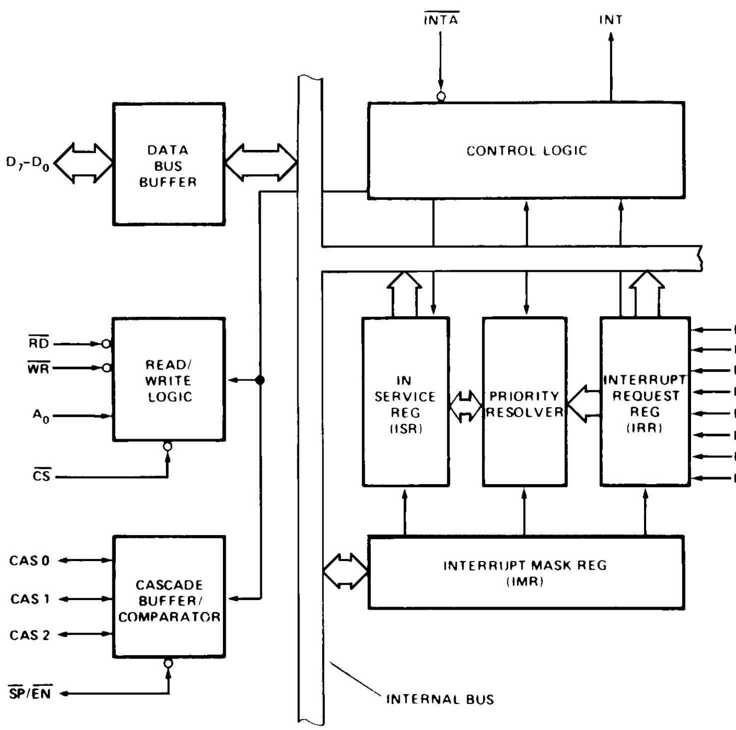
8259A
PROGRAMMABLE INTERRUPT CONTROLLER
(8259A/8259A-2)

- 8086, 8088 Compatible
- MCS-80, MCS-85 Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Available in 28-Pin DIP and 28-Lead PLCC Package
  (See Packaging Spec., Order #231369)
- Available in EXPRESS
  — Standard Temperature Range
  — Extended Temperature Range

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

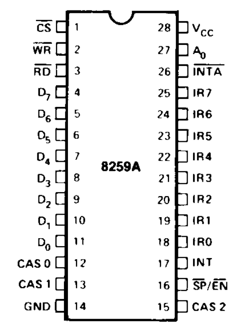
The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).



231468–1

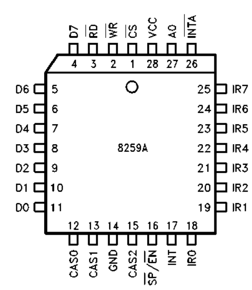
Figure 1. Block Diagram

DIP



231468–2

PLCC



231468–31

Figure 2. Pin Configurations

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7–D_0	4–11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**AO ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I.O devices such as keyboards, displays, sensors and other components receive servicing in a an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

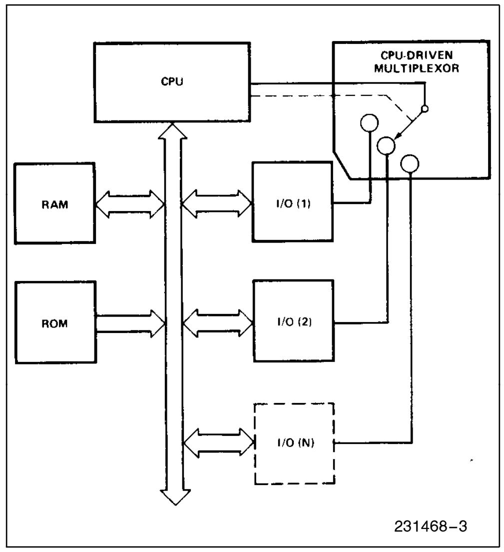


Figure 3a. Polled Method

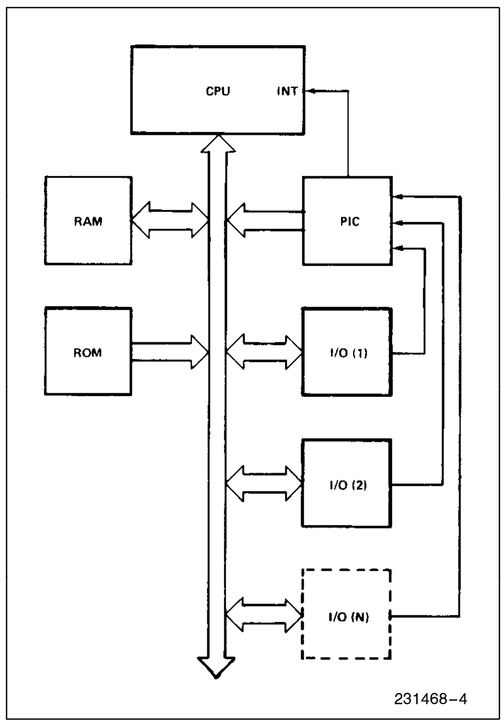


Figure 3b. Interrupt Method

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorites of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{\text{INTA}}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower quality.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{\text{INTA}}$ (INTERRUPT ACKNOWLEDGE)

$\overline{\text{INTA}}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{\text{CS}}$ (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{\text{WR}}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{\text{RD}}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

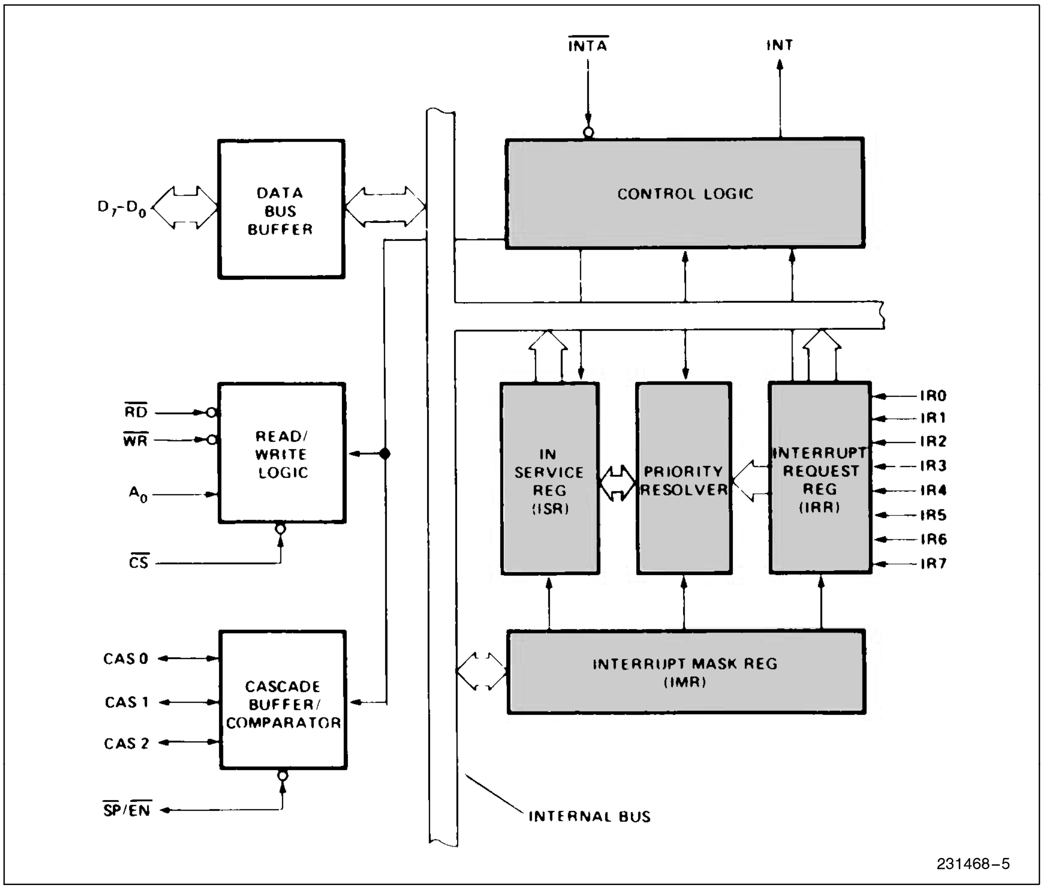


Figure 4a. 8259A Block Diagram

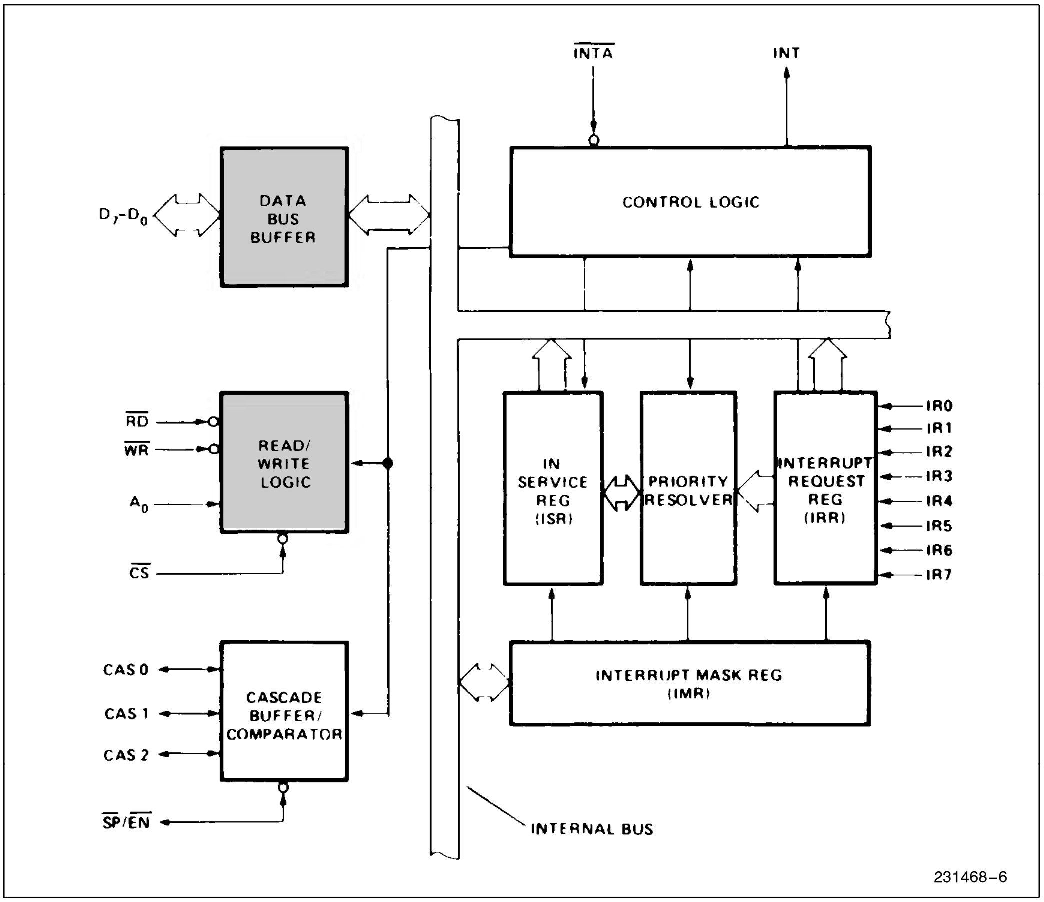


Figure 4b. 8259A Block Diagram

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0–2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses. (See section "Cascading the 8259A".)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7–0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7–0 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occuring in an 8086 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The 8086 will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

When the 8259A PIC receives an interrupt, INT becomes active and an interrupt acknowledge cycle is started. If a higher priority interrupt occurs between the two INTA pulses, the INT line goes inactive immediately after the second INTA pulse. After an unspecified amount of time the INT line is activated again to signify the higher priority interrupt waiting for service. This inactive time is not specified and can vary between parts. The designer should be aware of this consideration when designing a system which uses the 8259A. It is recommended that proper asynchronous design techniques be followed.

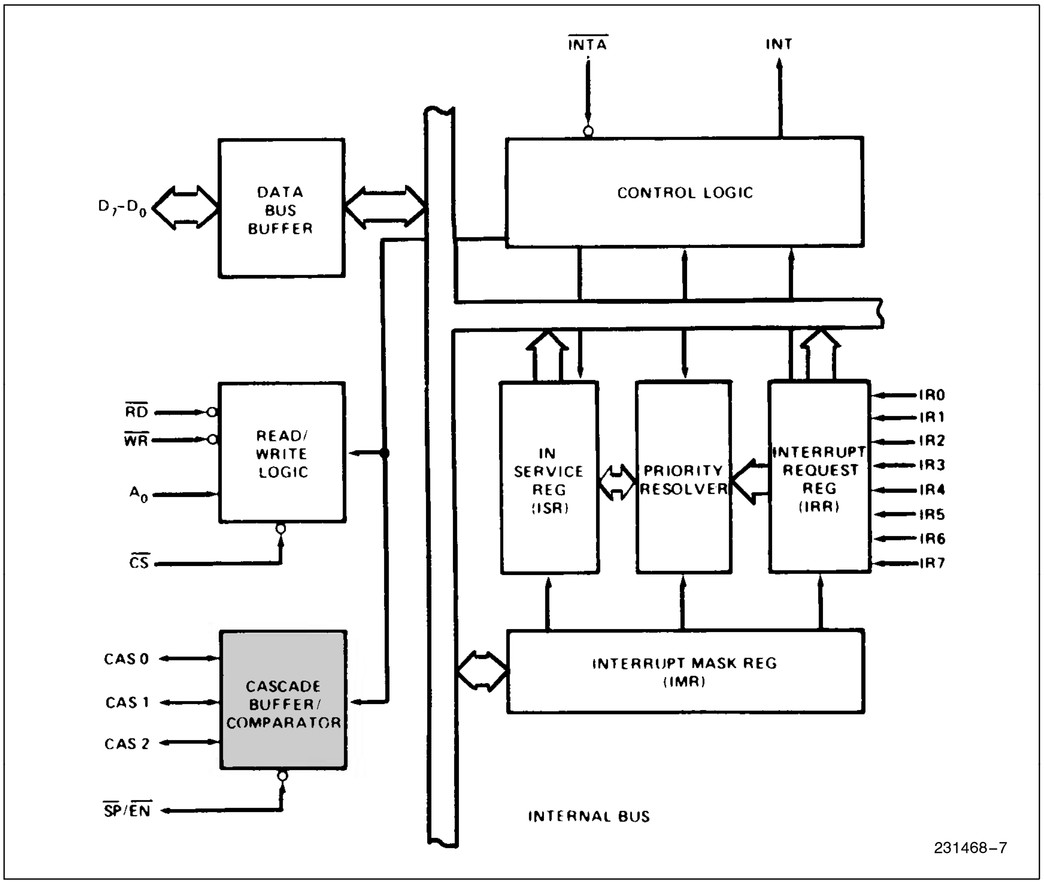


Figure 4c. 8259A Block Diagram

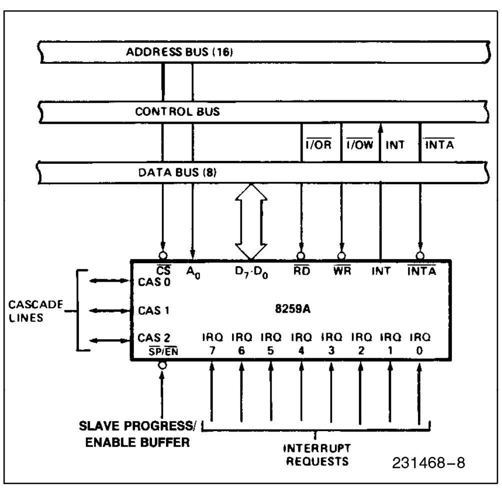


Figure 5. 8259A Interface to Standard System Bus

INTERRUPT SEQUENCE OUTPUTS

MCS-80, MCS-85

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5–A_7 are programmed, while A_0–A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0–A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{\text{INTA}}$ pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8–A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

8086, 8088

8086 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the $\overline{\text{INTA}}$ pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 8086 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5–A_{11} are unused in 8086 mode):

Content of Interrupt Vector Byte for 8086 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point—by a sequence of 2 to 4 bytes timed by $\overline{\text{WR}}$ pulses.
2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

General

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the intiitalization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transistion to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

d. The slave mode address is set to 7.

e. Special Mask Mode is cleared and Status Read is set to IRR.

f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

*NOTE:
Master/Slave in ICW4 is only used in the buffered mode.

Initialization Command Words 1 and 2 (ICW1, ICW2)

A_5–A_{15}: *Page starting address of service routines*. In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0–A_{15}). When the routine interval is 4, A_0–A_4 are automatically inserted by the 8259A, while A_5–A_{15} are programmed externally. When the routine interval is 8, A_0–A_5 are automatically inserted by the 8259A, while A_6–A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 8086 system A_{15}–A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}–A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set—ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 8086 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2–0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 8086) are released by it on the Data Bus.

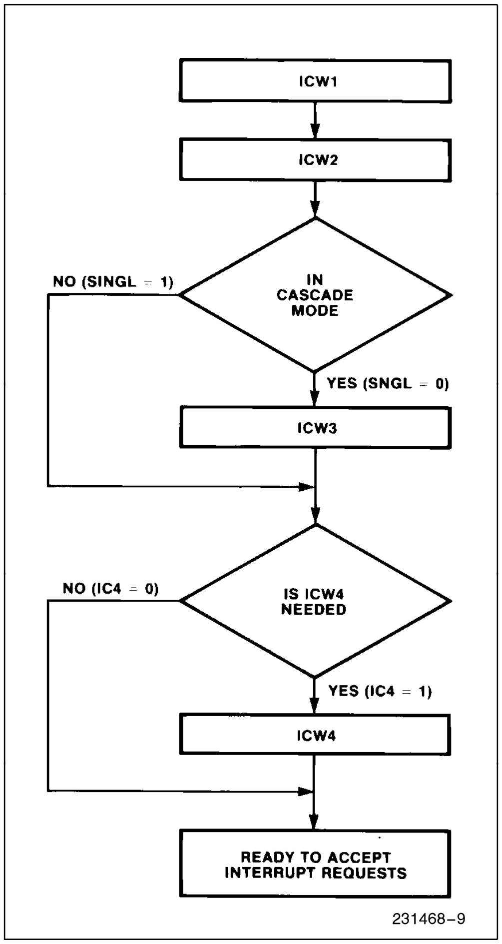


Figure 6. Initialization Sequence

Initialization Command Word 4 (ICW4)

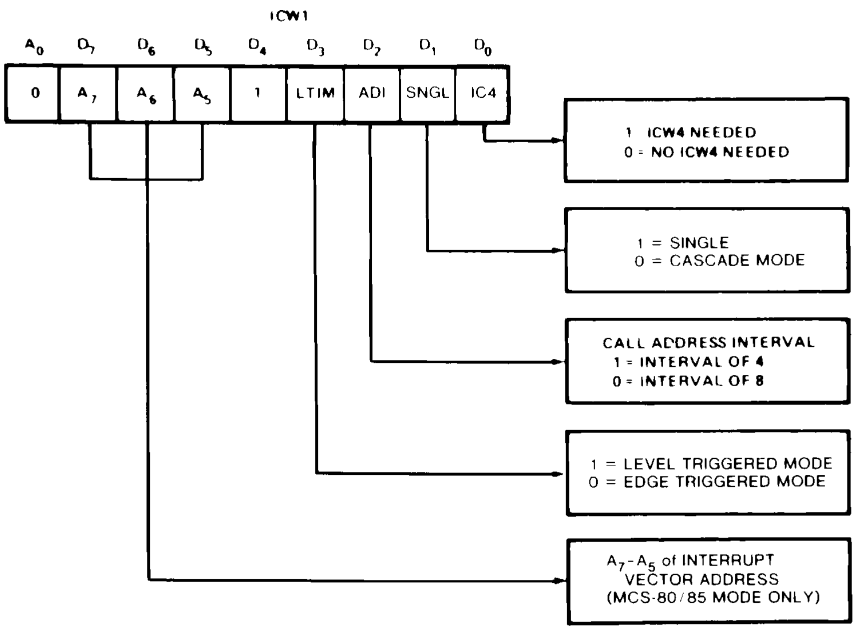
SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

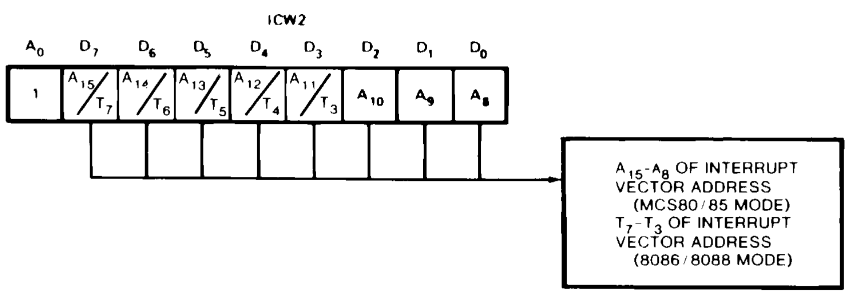
M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80, 85 system operation, μPM = 1 sets the 8259A for 8086 system operation.

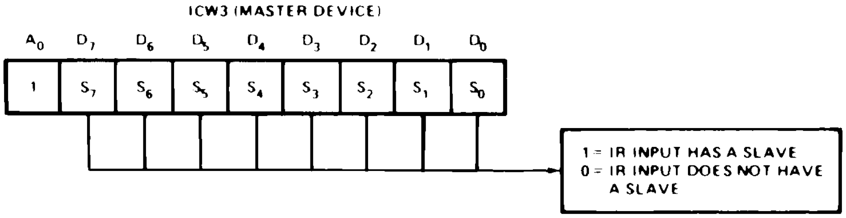


231468–10

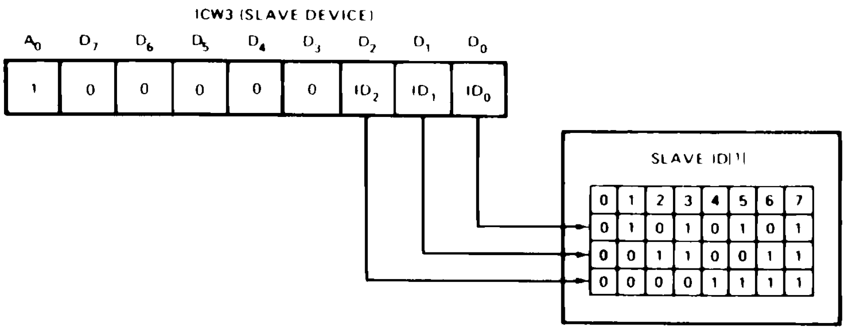


231468–11

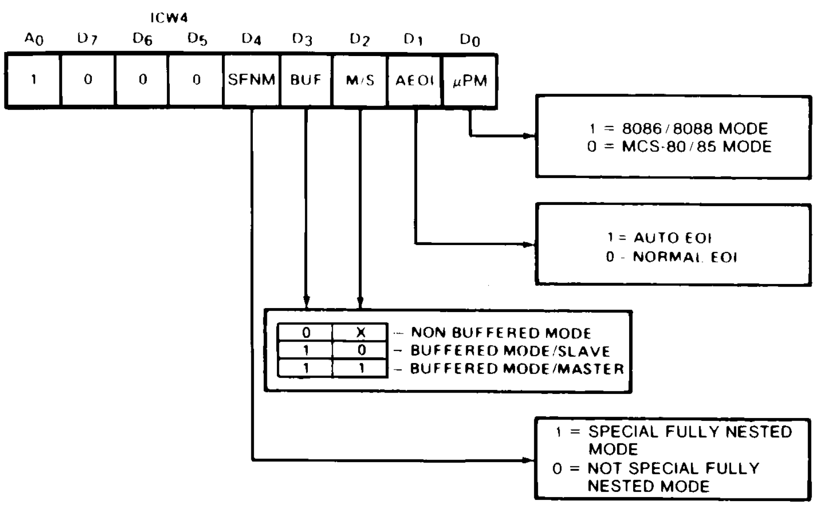
Figure 7. Initialization Command Word Format



231468–12



231468–13



231468–14

NOTE:
Slave ID is equal to the corresponding master IR input.

Figure 7. Initialization Command Word Format (Continued)

OPERATION COMMAND WORDS (OCWS)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

Operation Control Words (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SL	EOI	0	0	L2	L1	L0

OCW3

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	ESMM	SMM	0	1	P	RR	RIS

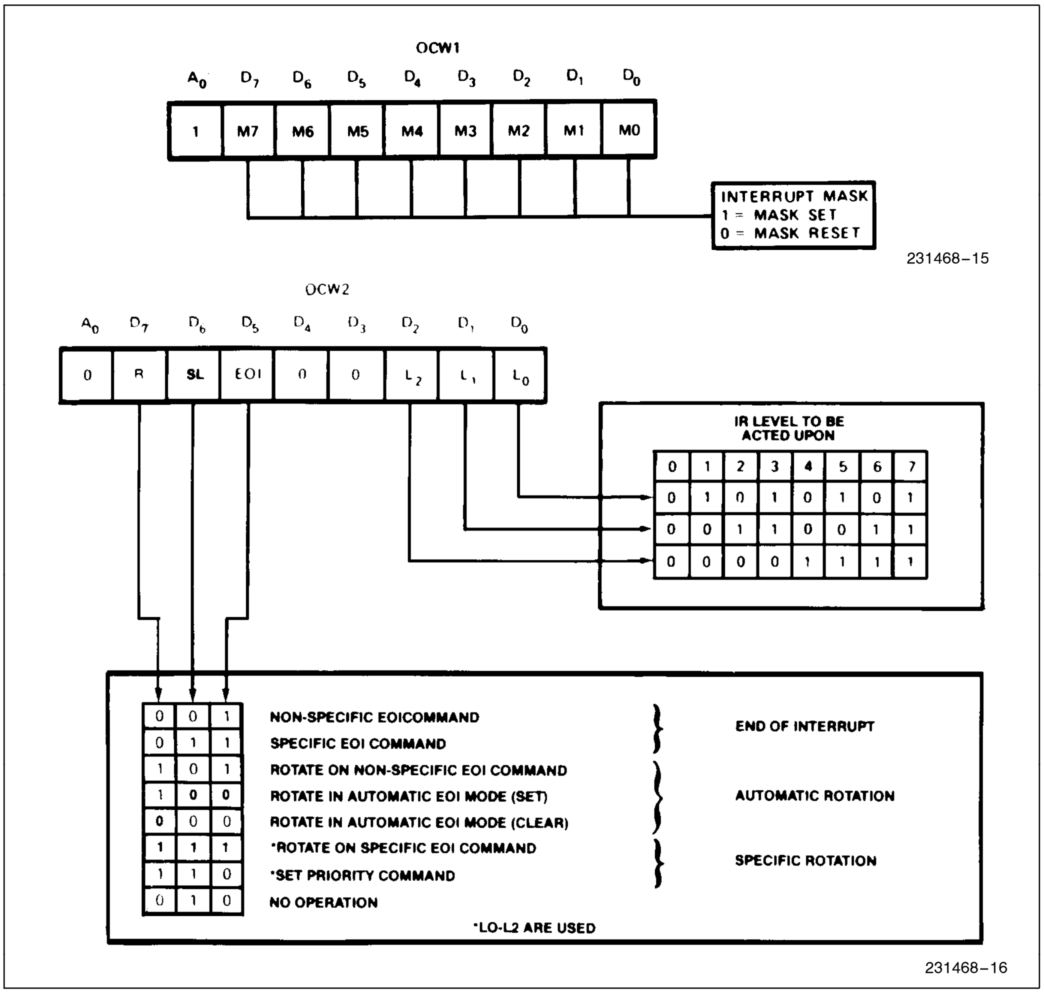


Figure 8. Operation Command Word Format

Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7–M_0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

Operation Control Word 2 (OCW2)

R, SL, EOI—These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.

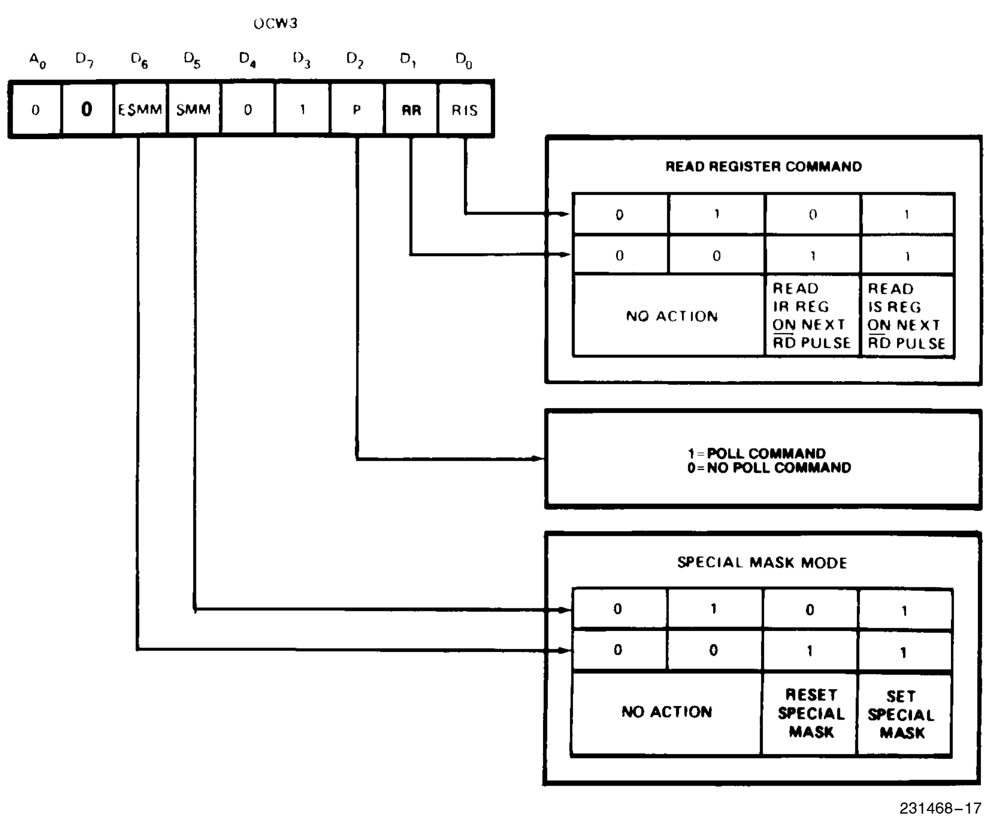


Figure 8. Operation Command Word Format (Continued)

Operation Control Word 3 (OCW3)

ESMM—Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM—Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest prioirity and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

End of Interrupt (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which perserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0–L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. in this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in 8086). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

The AEOI mode can only be used in a master 8259A and not a slave. 8259As with a copyright date of 1985 or later will operate in the AEOI mode as a master or a slave.

Automatic Rotation (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest prioirity requiring service)

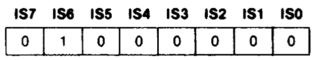
IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
0	1	0	1	0	0	0	0

"IS" Status 231468–18

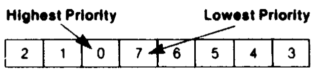
Lowest Priority							Highest Priority
7	6	5	4	3	2	1	0

Priority Status 231468–19

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)



"IS" Status 231468–20



Priority Status 231468–21

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1, L0–L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO–L2 = IR level to receive bottom priority).

Interrupt Masks

Each Interrupt Request input can bem masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OWC3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

Poll Command

In Poll mode the INT output functions as it normally does. The microprocessor should ignore this output. This can be accomplished either by not connecting the INT output or by masking interrupts within the microprocessor, thereby disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = '1" in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

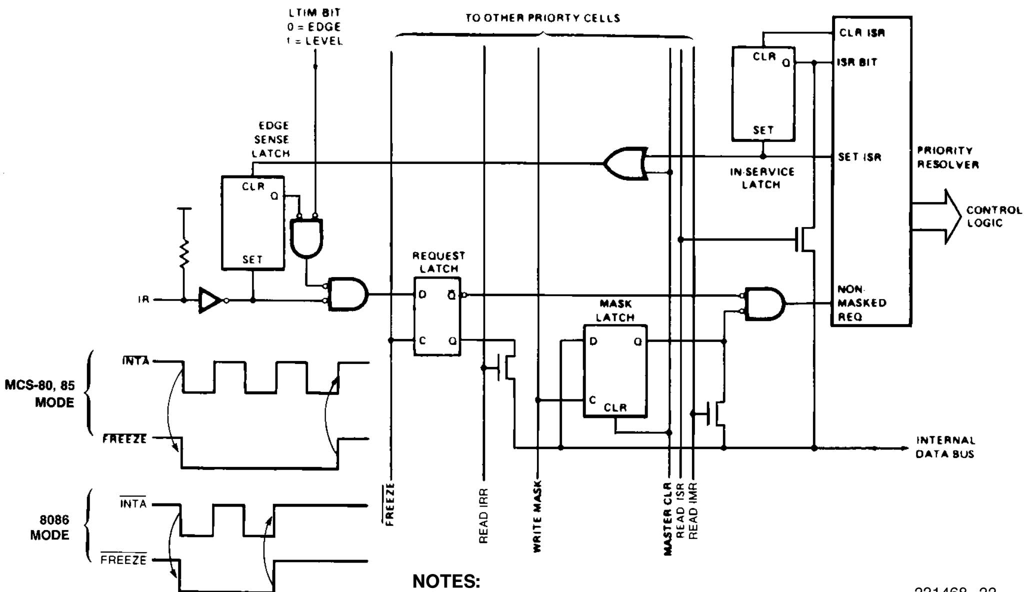
W0–W2: Binary code of the highest priority level requesting service.

I: Equal to "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

Reading the 8259A Status

The input status of several internal registers can be read to update the user information on the system.



NOTES:

231468–22

1. Master clear active only during ICW1.
2. $\overline{\text{FREEZE}}$ is active during $\overline{\text{INTA}}$ and poll sequences only.
3. Truth Table for a D-Latch.

C	D	Q	Operation
1	Di	Di	Follow
0	X	Qn-1	Hold

Figure 9. Priority Cell—Simplified Logic Diagram

The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read, when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{\text{RD}}$ is active and A0 = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

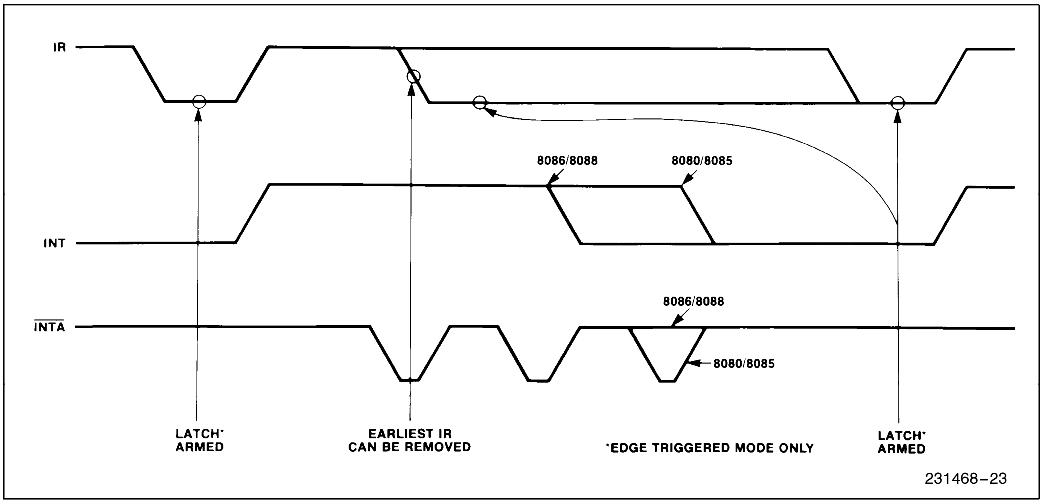


Figure 10. IR Triggering Timing Requirements

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupts is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first $\overline{\text{INTA}}$. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

The Special Fully Nest Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

Buffered Mode

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{\text{SP}}/\overline{\text{EN}}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{\text{SP}}/\overline{\text{EN}}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low).

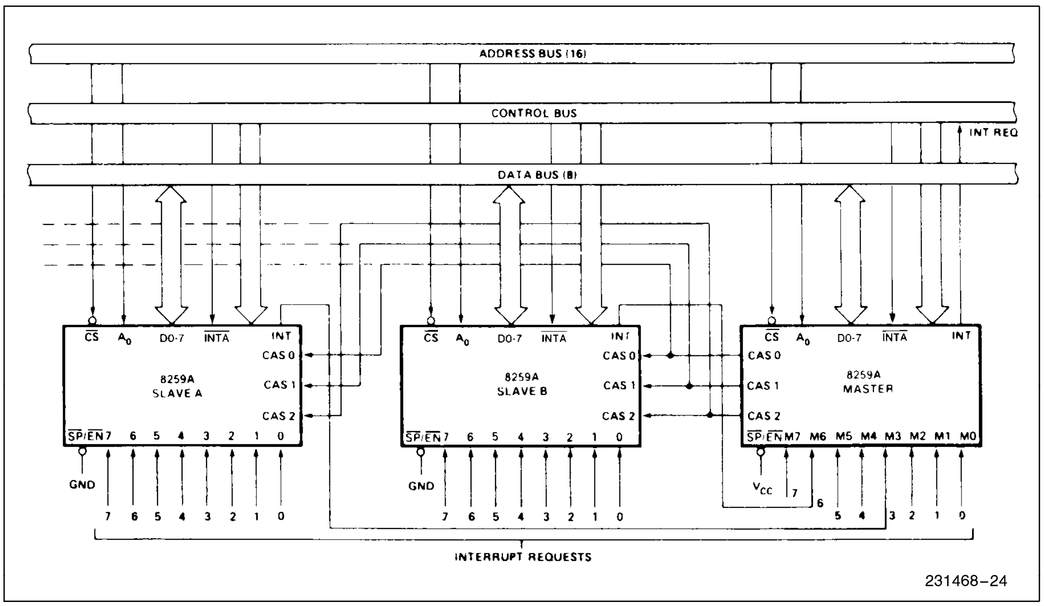


Figure 11. Cascading the 8259A

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . . 0°C to 70°C

Storage Temperature . . . . −65°C to +150°C

Voltage on Any Pin
with Respect to Ground . . . . −0.5V to +7V

Power Dissipation 1W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0*	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = −100 μA
		2.4		V	I_{OH} = −400 μA
I_{LI}	Input Load Current	−10	+10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LOL}	Output Leakage Current	−10	+10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		−300	μA	V_{IN} = 0
			10	μA	V_{IN} = V_{CC}

***NOTE:**
For Extended Temperature EXPRESS V_{IH} = 2.3V.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to V_{SS}

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

Symbol	Parameter	8259A		8259A-2		Units	Test Conditions
		Min	Max	Min	Max		
TAHRL	AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$ ↓	0		0		ns	
TRHAX	AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$ ↑	0		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	235		160		ns	
TAHWL	AO/$\overline{CS}$ Setup to $\overline{WR}$ ↓	0		0		ns	
TWHAX	AO/$\overline{CS}$ Hold after $\overline{WR}$ ↑	0		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	290		190		ns	
TDVWH	Data Setup to $\overline{WR}$ ↑	240		160		ns	
TWHDX	Data Hold after $\overline{WR}$ ↑	0		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ ↓ (Slave Only)	55		40		ns	
TRHRL	End of $\overline{RD}$ to Next $\overline{RD}$ End of $\overline{INTA}$ to Next $\overline{INTA}$ within an $\overline{INTA}$ Sequence Only	160		100		ns	
TWHWL	End of $\overline{WR}$ to Next $\overline{WR}$	190		100		ns	
*TCHCL	End of Command to Next Command (Not Same Command Type)	500		150		ns	
	End of $\overline{INTA}$ Sequence to Next $\overline{INTA}$ Sequence.	500		300			

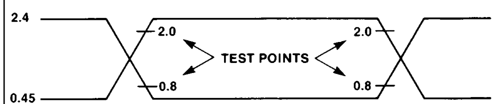
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6 µs, 8085A-2 = 1 µs, 8086 = 1 µs, 8086-2 = 625 ns)

NOTE:
This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

Symbol	Parameter	8259A		8259A-2		Units	Test Conditions
		Min	Max	Min	Max		
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$ ↓		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$ ↑	10	100	10	85	ns	C of Data Bus Max Test C = 100 pF Min Test C = 15 pF
TJHIH	Interrupt Output Delay		350		300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$ ↓ (Master Only)		565		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$ ↓ or $\overline{INTA}$ ↓		125		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$ ↑ or $\overline{INTA}$ ↑		150		150	ns	
TAHDV	Data Valid from Stable Address		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		200	ns	

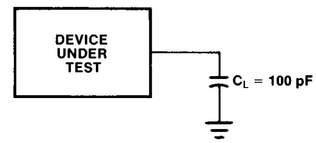
A.C. TESTING INPUT/OUTPUT WAVEFORM



231468–25

A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

A.C. TESTING LOAD CIRCUIT

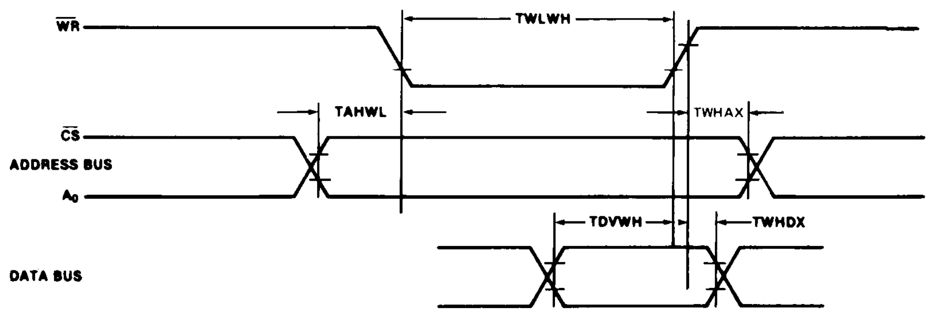


231468–26

C_L = 100 pF
C_L Includes Jig Capacitance

WAVEFORMS

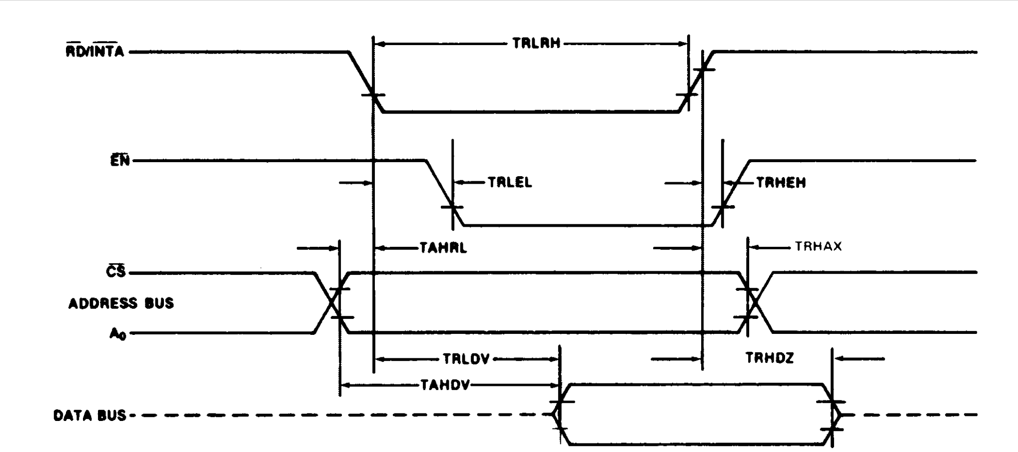
WRITE



231468–27

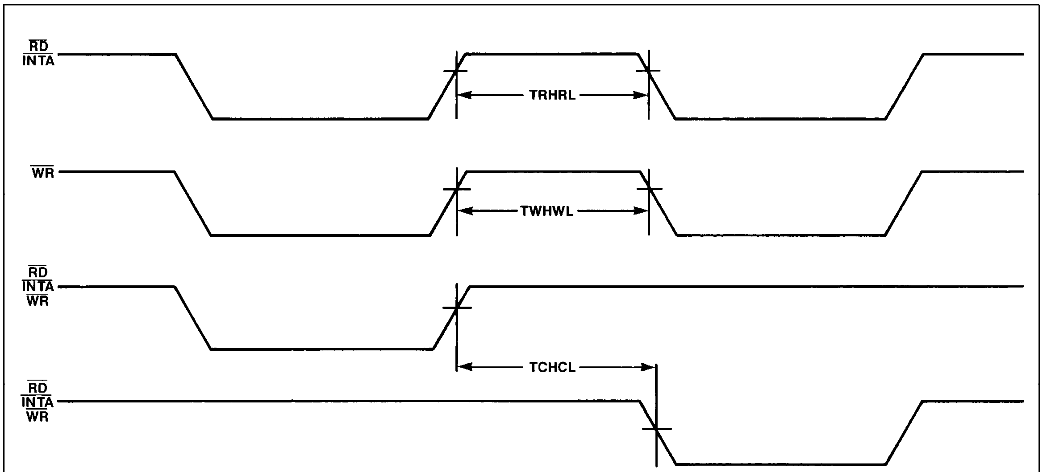
WAVEFORMS (Continued)

READ/INTA



231468–28

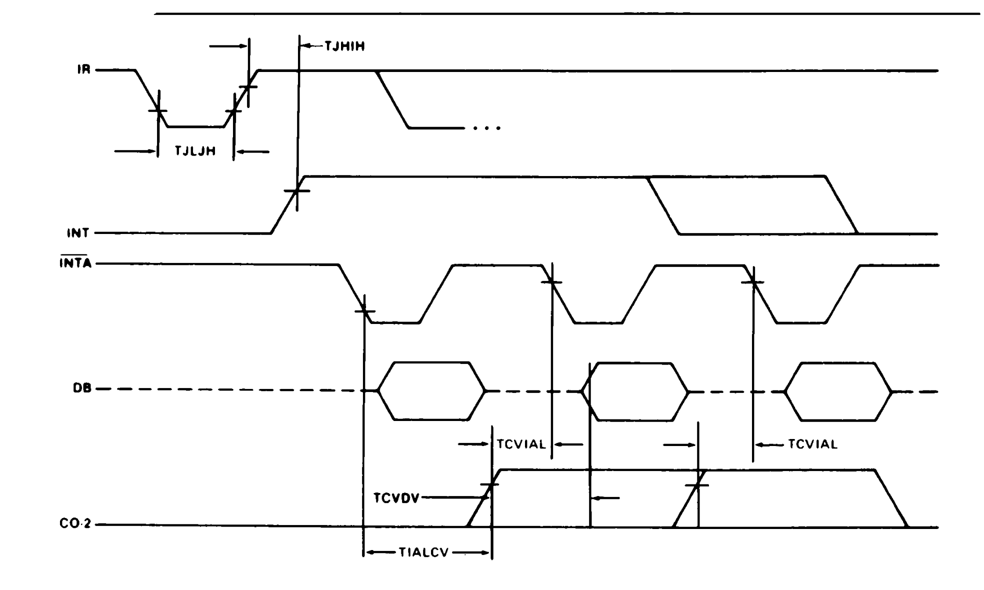
OTHER TIMING



231468–29

WAVEFORMS (Continued)

$\overline{\text{INTA}}$ SEQUENCE



NOTES:
Interrupt output must remain HIGH at least until leading edge of first $\overline{\text{INTA}}$.
1. Cycle 1 in 8086, 8088 systems, the Data Bus is not active.

Data Sheet Revision Review

The following changes have been made since revision 2 of the 8259A data sheet.

1. The first paragraph of the Poll Command section was rewritten to clarify the status of the INT pin.
2. A paragraph was added to the Interrupt Sequence section to indicate the status of the INT pin during multiple interrupts.
3. A reference to PLCC packaging was added.
4. All references to the 8259A-8 have been deleted.

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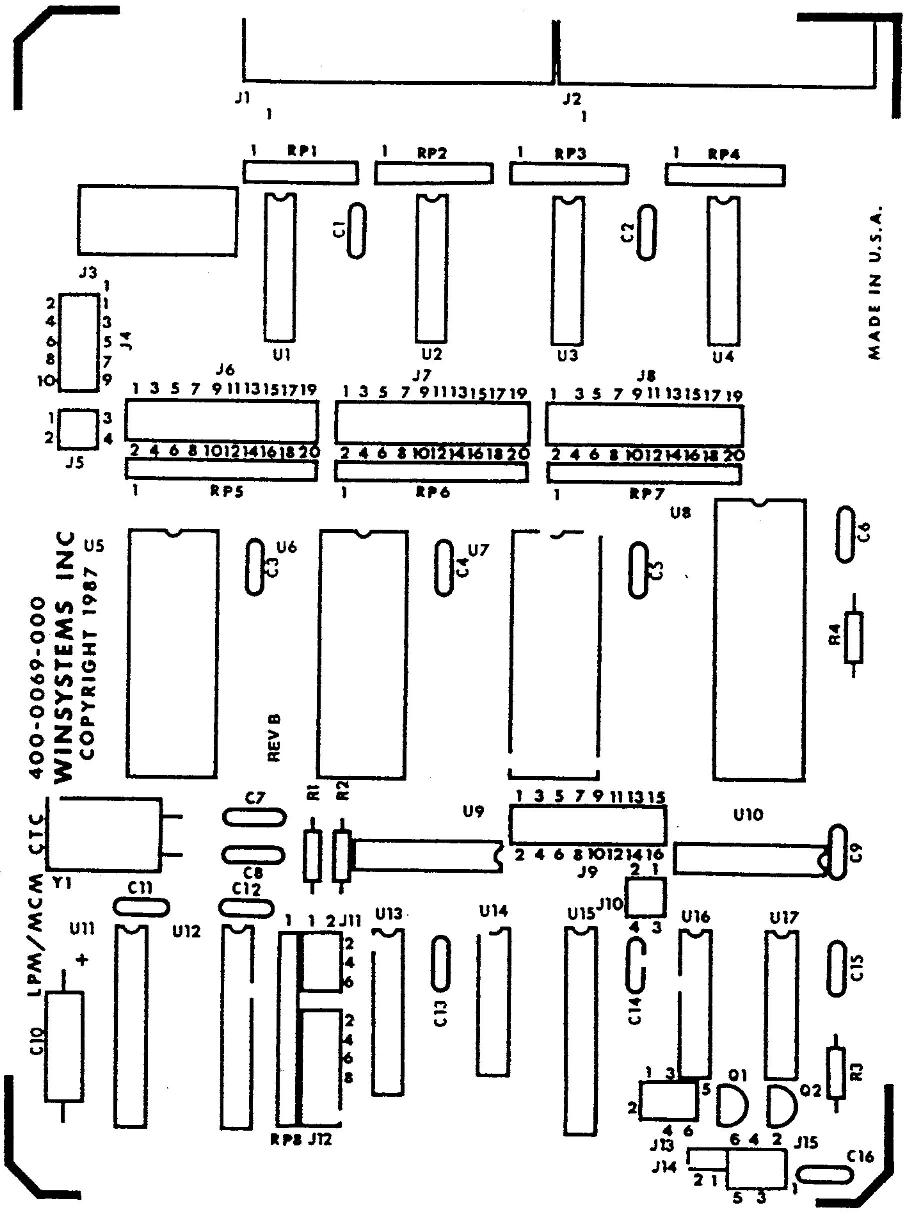
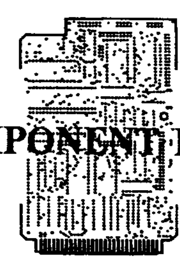




COMPONENT LAYOUT

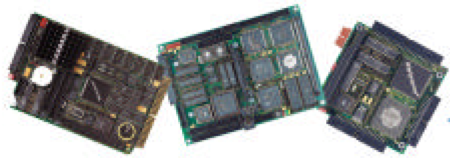
LPM/MCM-CTC REV B

BEGINNING RANGE: MCM-CTC-0 ENDING RANGE: MCM-CTC-1

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	MCM-CTC-0	COUNTER/TIMER CARD					1
2	0069-200-0000	ASSY MCM-CTC-0 REV B	ASSY MCM-CTC-0 REV B	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	04-04-91 ADD ECO 91-04	ARLIN		Inv	1
3	>109-1001-000	WIRE JUMPER .1 SPACE BARE	INSTALL IN HOLES FOR EMITTER	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	& BASE OF Q2	ARLIN		Inv	1
3	>110-0001-001	CAP 22PF MICA RAD CM05ED220J03	C7,C8	ARLIN		Inv	2
3	>110-0010-003	CAP .1 UF CER RAD SR215E104MAA	C1-C6,C9,C11-C16	ARLIN		Inv	13
3	>110-0017-002	CAP 22 UF ALU ELEC AX TLB1C220M	C10	ARLIN		Inv	1
3	>114-0102-450	RESISTOR 1K 1/4 5%	R1,R3	ARLIN		Inv	2
3	>114-0105-450	RESISTOR 1.0M 1/4 5%	R2	ARLIN		Inv	1
3	>115-0103-050	RN SIP 6P-5 RES 10K SRDSA-06P-C1	RP1-RP4	ARLIN		Inv	4
3	>117-0103-050	RN SIP 10P-9 RES 10K CSC10A01103	RP5-RP8	ARLIN		Inv	4
3	>125-0003-000	TRANSISTOR VN2222LL	Q1	ARLIN		Inv	1
3	>200-0246-100	SOCKET 24 P .6 ICO-246-S8A-T (10	U5-U7	ARLIN		Inv	3
3	>201-0010-121	HDR 2X5 RA PRO IDH-10LP-SR3-TG/T	J3	ARLIN		Inv	1
3	>201-0026-121	HDR 26 POS RA IDH-26LP-SR3-TG/TR	J1,J2	ARLIN		Inv	2
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J4=2X5,J5,J10	ARLIN		Inv	1.722
3	>999-9999-001	SPECIAL NOTES	J6-J8=2X10,J9=2X8,	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J11,J13,J15=2X3,J12=2X6,J14=2X1	ARLIN		Inv	1
3	>220-0005-000	XTAL 4.91520 20 PF U18-20-49	Y1 INSTALL FOAM TAPE UNDER	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	XTAL	ARLIN		Inv	1
3	>340-0008-100	IC, 74LS08	U16	ARLIN		Inv	1
3	>340-0032-100	IC, 74LS32	U14	ARLIN		Inv	1
3	>340-0074-100	IC, 74LS74	U17	ARLIN		Inv	1
3	>340-0138-100	IC, 74LS138	U13	ARLIN		Inv	1
3	>340-0244-100	IC, 74LS244	U15	ARLIN		Inv	1
3	>340-0245-100	IC, 74LS245	U11	ARLIN		Inv	1
3	>340-0393-100	IC, 74LS393	U10	ARLIN		Inv	1
3	>340-0688-100	IC, 74LS688	U12	ARLIN		Inv	1
3	>400-0069-000	PCB CTC REV B (T)	PCB CTC REV B (T)	ARLIN		Inv	1
3	>500-0001-000	EJECTOR SCANBE S208	STAMP (RED) CTC	ARLIN		Inv	1
3	>500-0002-000	ROLL PIN		ARLIN		Inv	1
3	>741-0004-200	IC, 74HC04	U9	ARLIN		Inv	1
3	>741-0014-200	IC, 74HC14	U1-U4	ARLIN		Inv	4
3	>999-9999-001	SPECIAL NOTES	R4 USER OPTION (MASK OFF)	ARLIN		Inv	1
2	0069-400-0000	SUB ASSY LPM/MCM-CTC-0 REV B	SUB ASSY LPM/MCM-CTC-0 REV B	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	3-01-91	ARLIN		Inv	1
3	>201-0002-000	PLUG JUMPER 999-19-310-00	J10=3-4, J6=2-4 7-8 9-10	ARLIN		Inv	25
3	>999-9999-001	SPECIAL NOTES	13-14 15-16 19-20, J7,J8=	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	3-4 7-8 9-10 13-14 15-16	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	19-20, J13=1-2 3-4 5-6,	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J15=3-4, J9=7-8 15-16	ARLIN		Inv	1
3	>801-0030-200	IC, 71054C TIMER CMOS	U5-U7	ARLIN		Inv	3
2	950-0001-000	BAG ANTISTATIC 6X10 CHARLES WATE	BAG ANTISTATIC 6X10 CHARLES WATER CP303	ARLIN		Inv	1

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	MCM-CTC-1	CTC-0 WITH 8259A INTER.CONTROL					1
2	0069-210-0000	ASSY MCM-CTC-1 REV B	ASSY MCM-CTC-1 REV B	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	04-04-91 ADD ECO 91-04	ARLIN		Inv	1
3	>110-0001-001	CAP 22PF MICA RAD CM05ED220J03	C7,C8	ARLIN		Inv	2
3	>110-0010-003	CAP .1 UF CER RAD SR215E104MAA	C1-C6,C9,C11-C16	ARLIN		Inv	13
3	>110-0017-002	CAP 22 UF ALU ELEC AX TLB1C220M	C10	ARLIN		Inv	1
3	>114-0102-450	RESISTOR 1K 1/4 5%	R1,R3	ARLIN		Inv	2
3	>114-0105-450	RESISTOR 1.0M 1/4 5%	R2	ARLIN		Inv	1
3	>115-0103-050	RN SIP 6P-5 RES 10K SRDSA-06P-C1	RP1-RP4	ARLIN		Inv	4
3	>117-0103-050	RN SIP 10P-9 RES 10K CSC10A01103	RP5-RP8	ARLIN		Inv	4
3	>125-0003-000	TRANSISTOR VN2222LL	Q1,Q2	ARLIN		Inv	2
3	>200-0246-100	SOCKET 24 P .6 ICO-246-S8A-T (10	U5-U7	ARLIN		Inv	3
3	>200-0286-100	SOCKET 28 P .6 ICO-286-S8A-T (18	U8	ARLIN		Inv	1
3	>201-0010-121	HDR 2X5 RA PRO IDH-10LP-SR3-TG/T	J3	ARLIN		Inv	1
3	>201-0026-121	HDR 26 POS RA IDH-26LP-SR3-TG/TR	J1,J2	ARLIN		Inv	2
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J4=2X5,J5,J10	ARLIN		Inv	1.722
3	>999-9999-001	SPECIAL NOTES	J6-J8=2X10,J9=2X8,	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J11,J13,J15=2X3,J12=2X6,J14=2X1	ARLIN		Inv	1
3	>220-0005-000	XTAL 4.91520 20 PF U18-20-49	Y1 INSTALL FOAM TAPE UNDER	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	XTAL	ARLIN		Inv	1
3	>340-0008-100	IC, 74LS08	U16	ARLIN		Inv	1
3	>340-0032-100	IC, 74LS32	U14	ARLIN		Inv	1
3	>340-0074-100	IC, 74LS74	U17	ARLIN		Inv	1
3	>340-0138-100	IC, 74LS138	U13	ARLIN		Inv	1
3	>340-0244-100	IC, 74LS244	U15	ARLIN		Inv	1
3	>340-0245-100	IC, 74LS245	U11	ARLIN		Inv	1
3	>340-0393-100	IC, 74LS393	U10	ARLIN		Inv	1
3	>340-0688-100	IC, 74LS688	U12	ARLIN		Inv	1
3	>400-0069-000	PCB CTC REV B (T)	PCB CTC REV B (T)	ARLIN		Inv	1
3	>500-0001-000	EJECTOR SCANBE S208	STAMP (RED) CTC	ARLIN		Inv	1
3	>500-0002-000	ROLL PIN		ARLIN		Inv	1
3	>741-0004-200	IC, 74HC04	U9	ARLIN		Inv	1
3	>741-0014-200	IC, 74HC14	U1-U4	ARLIN		Inv	4
3	>999-9999-001	SPECIAL NOTES	R4 USER OPTION	ARLIN		Inv	1
2	0069-410-0000	SUB ASSY LPM/MCM-CTC-1 REV B	SUB ASSY LPM/MCM-CTC-1 REV B	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	3-01-91	ARLIN		Inv	1
3	>201-0002-000	PLUG JUMPER 999-19-310-00	J6=2-4 7-8 9-10 13-14 15-16	ARLIN		Inv	25
3	>999-9999-001	SPECIAL NOTES	19-20, J7,J8= 3-4 7-8 9-10	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	13-14 15-16 19-20,	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J9=7-8 15-16, J10=3-4,	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J13=1-2 3-4 5-6, J15=3-4	ARLIN		Inv	1
3	>801-0030-200	IC, 71054C TIMER CMOS	U5-U7	ARLIN		Inv	3
3	>801-0035-200	IC, 71059C INT CNTL CMOS	U8	ARLIN		Inv	1
2	950-0001-000	BAG ANTISTATIC 6X10 CHARLES WATE	BAG ANTISTATIC 6X10 CHARLES WATER CP303	ARLIN		Inv	1

WARRANTY AND REPAIR INFORMATION



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The customer must send the product freight prepaid and insured. The product must be enclosed in an anti-static bag to protect it from damage caused by static electricity. Each bag must be completely sealed. Packing material must separate each unit returned and placed as a cushion between the unit(s) and the sides and top of the shipping container. WinSystems is not responsible for any damage to the product due to inadequate packaging or static electricity.