

OPERATIONS MANUAL

PCM-I/O48

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REVISION HISTORY

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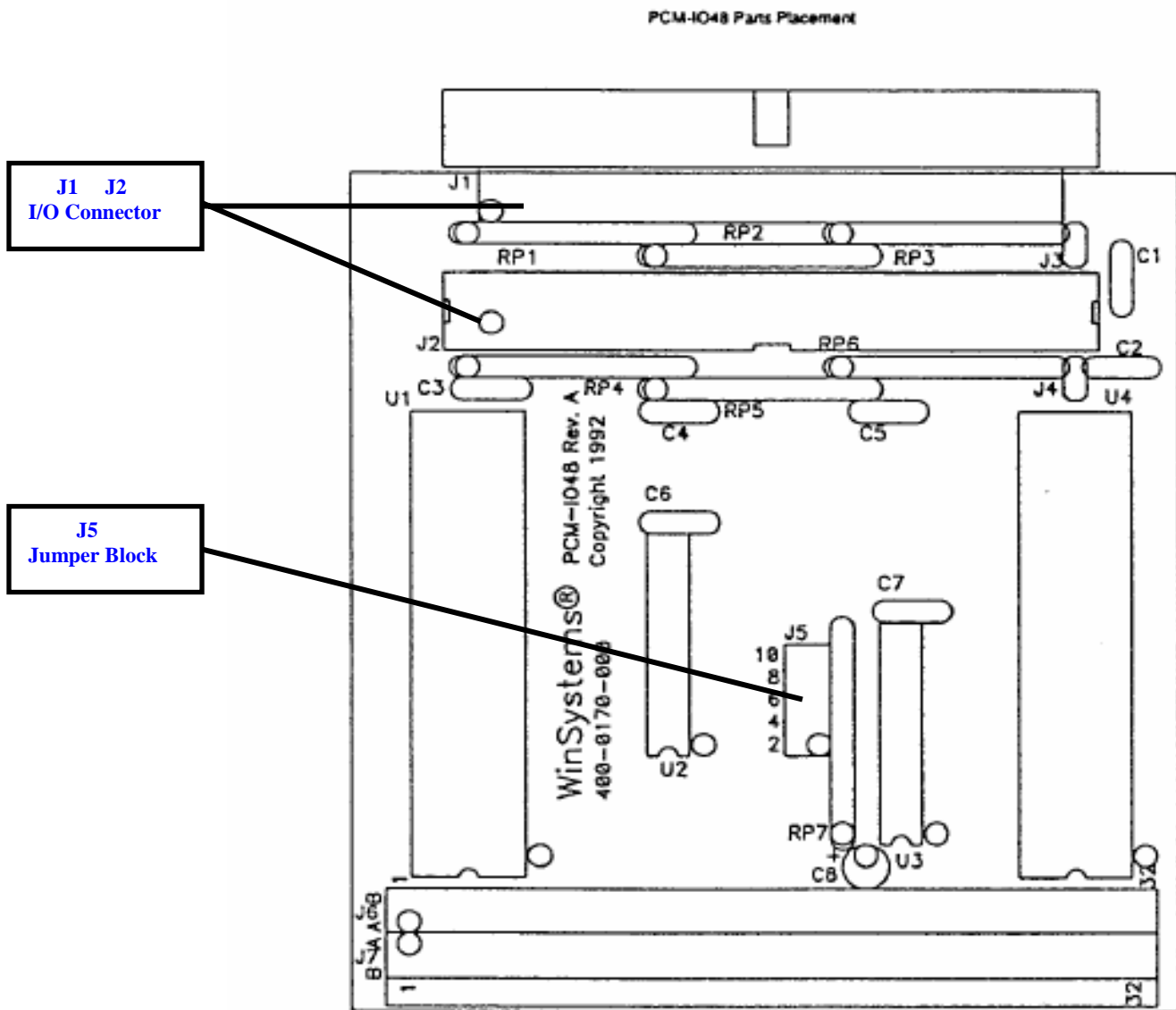
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TABLE OF CONTENTS

Section	Paragraph Title	Page
	Visual Index – Quick Reference	i
1	General Information	1-1
1.1	Features	1-1
1.2	Functional Capability	1-1
1.3	Specifications	1-3
2	User Information	2-1
2.1	I/O Addressing	2-1
2.2	Connector Pin-Outs	2-2
2.3	Programming	2-3
	APPENDIX Datasheet Reprint, Cable Drawings, Software Examples	
	Warranty Statement	

Visual Index – Quick Reference

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



1 General Information

1.1 Features

- 48 I/O lines configured as six, 8-bit parallel I/O ports
- Designed to interface directly to 2 standard industrial isolated I/O module racks (Opto-22)
- Dual 50-pin header connectors
- Single 8-bit PC/104 module compatible
- Uses two 82C55A (NEC 71055) PPIs
- No power glitching on I/O lines
- Single +5 volt operation
- Extended operational temperature range -40 ° to + 85 ° Centigrade

The PCM-IO48 is a low cost, general purpose, PC/104 compatible 48-line parallel I/O controller based upon two 82C55A integrated circuits. The I/O lines are organized as two groups of three, 8-bit I/O ports. It is wired to two, 50-pin connectors which each will interface directly to industry standard 4, 8, 16 and 24-I/O module solid state relay mounting racks (Opto-22, etc.).

The PCM-IO48 is small, only 3.6" x 3.8". It is an 8-bit, stack through module that can be used in a standalone stack or as a mezzanine bus stacked atop a larger single board computer like the WinSystems' EBC, LBC PCM, and SAT series of embedded PCs. It will operate over the full industrial temperature range of -40°C to +85°C.

1.2 FUNCTIONAL CAPABILITY

PC/104 Interface - The PCM-IO48 is I/O port mapped. The I/O address is jumper selectable for 16 different addresses on eight byte boundaries. The range is from 0100H to 0178H.

Parallel Controller - Two 82C55A Programmable Peripheral Interface (PPI) devices are on the PCM-IO48 board. Each chip is independent from the other and each supports 24 I/O pins.

In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking. The third mode of operation (Mode 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, plus 5 lines for handshaking.

Although an 82C55A offers great flexibility as a general purpose parallel interface device, it can be programmed in Mode 0 for use with standard I/O mounting racks. This means that the digital signal conditioning modules must be grouped in sets of 4 as either input or output.

The signal levels are TTL compatible. Each I/O line has a 10K ohm pull-up resistor to keep the input from floating.

I/O Connector - Each 82C55A has its 24 I/O lines connected to a separate 50-pin connector. The 24 data lines are alternated with 24 ground lines for reduced noise and crosstalk. Also +5 volts and ground are included in the cable. The pinout is compatible with the industry standard 4 to 24 position I/O module mounting racks (Opto-22, etc.) for use with high level AC and DC opto-isolated solid state relays.

A 50 conductor ribbon cable such as the WinSystems' CBL-115-4 connects the PCM-IO48 to one I/O rack. Two cables are required to fully utilize this card, one for each rack. The cable will interface directly to a 4, 8, 16 or 24 module rack.

1.3 SPECIFICATIONS

Electrical

PC/104 Bus: 64-pin 0.100" socket 8-bit, stack through
Parallel Interface: 48 I/O lines, TTL compatible
Power Requirements: +5V \pm 10% @ 20mA typ.

Mechanical

Dimensions: 3.6" x 3.8" (90mm x 96mm)
Weight: 3.36 oz.

Connectors

Parallel: Two, 50-pin dual 0.100" headers
Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85C
Non-condensing relative humidity: 5% to 95%
MTBF: 63.3 years

2 User Information

2.1 I/O Addressing – The PCM-IO48 uses an EPAL for I/O address decoding. The starting address for the board is controlled by Jumper block J5. Each decoded I/O address block takes eight I/O addresses. The address decoder is programmed for 16 different starting addresses that range for 0100H to 0178H on eight byte boundaries.

NOTE: The I/O ports associated with connector J1, begin at the **BASE_ADDRESS + 4**, the I/O ports for J2 begin at **BASE_ADDRESS + 0**.

TABLE 2-1
J5 JUMPER BLOCK I/O ADDRESSING
STARTING BASE ADDRESSES

100H	108H	110H	118H	120H	128H
1o--o2	1o o2	1o--o2	1o o2	1o--o2	1o o2
3o--o4	3o--o4	3o o4	3o o4	3o--o4	3o--o4
5o--o6	5o--o6	5o--o6	5o--o6	5o o6	5o o6
7o--o8	7o--o8	7o--o8	7o--o8	7o--o8	7o--o8
9o o10	9o o10	9o o10	9o o10	9o o10	9o o10
130H	138H	140H	148H	150H	158H
1o--o2	1o o2	1o--o2	1o o2	1o--o2	1o o2
3o o4	3o o4	3o--o4	3o--o4	3o o4	3o o4
5o o6	5o o6	5o--o6	5o--o6	5o--o6	5o--o6
7o--o8	7o--o8	7o o8	7o o8	7o o8	7o o8
9o o10	9o o10	9o o10	9o o10	9o o10	9o o10
160H	168H	170H	178H		
1o--o2	1o o2	1o--o2	1o o2		
3o--o4	3o--o4	3o o4	3o o4		
5o o6	5o o6	5o o6	5o o6		
7o o8	7o o8	7o o8	7o o8		
9o o10	9o o10	9o o10	9o o10		

NOTE: J5 9-10 MUST BE LEFT OPEN AND IS FOR BOARD TEST ONLY

J2 I/O address: **BASE_ADDRESS + 0**

J1 I/O address: **BASE_ADDRESS + 4**

2.2 Connector Pin-Outs - The PCM-IO48 consists of two 8255/82C55 (NEC 70155) Programmable Peripheral Interface (PPI) devices. Each PPI device has 24 lines of parallel that can be programmed for three different modes of operation. All of the parallel I/O lines from each PPI have a 10K pull-up resistor and is brought out to one of the two 50 pin connectors on the board. The mating connector for J1 and J2 is a Panduit 050-050-455 or equivalent.

NOTE: For applications that require boards to be stacked on top of the PCM-I/O48, it will not be possible to use a strain relief on connector J2.

J1 and J2 - Rack I/O Connector

Pin	Description	Pin	Description
1	PA0	2	Gnd
3	PA1	4	Gnd
5	PA2	6	Gnd
7	PA3	8	Gnd
9	PA4	10	Gnd
11	PA5	12	Gnd
13	PA6	14	Gnd
15	PA7	16	Gnd
17	PB0	18	Gnd
19	PB1	20	Gnd
21	PB2	22	Gnd
23	PB3	24	Gnd
25	PB4	26	Gnd
27	PB5	28	Gnd
29	PB6	30	Gnd
31	PB7	32	Gnd
33	PC0	34	Gnd
35	PC1	36	Gnd
37	PC2	38	Gnd
39	PC3	40	Gnd
41	PC4	42	Gnd
43	PC5	44	Gnd
45	PC6	46	Gnd
47	PC7	48	Gnd
49	+5v	50	Gnd

2.3 Programming – Programming the PCM-I/O48 consists of outputting several command words to the PPI device that is to be used. The I/O address of the PCM-I/O48 is controlled by the jumper block J5. The PCM-I/O48 powers up in MODE 0 with all lines set to inputs. Most PCM-I/O48 applications will use Mode 0 for input and output operations. Port 0 and Port 1 of the 71055 can be only accessed as bytes whereas Port 2 can be accessed as upper and lower 4 bits. See the following programming example for an example of how to initialize the 71055 for Ports 0, 1, and 2. For programming and examples for the 70155 (82C55) the user should consult the appendix for further information.

```

/* Sample 8255 initialization for PCM-I/O48 */

/* Define Addresses of the Data and Command Ports */

#define PORT_BASE 0x100          /* Board addressed at 100 Hex */

#define PI01_A          PORT_BASE
#define PI01_B          PORT_BASE + 1
#define PI01_C          PORT_BASE + 2
#define PI01_CMD        PORT_BASE + 3

#define PI02_A          PORT_BASE + 4
#define PI02_B          PORT_BASE + 5
#define PI02_C          PORT_BASE + 6
#define PI02_CMD        PORT_BASE + 7

/* Group 1 direction commands */

#define PORT2_IN_LSB    0x01          /* LSB of port 2 for input */
#define PORT2_OUT_LSB   0x00          /* LSB of port 2 for output */
#define PORT1_IN        0x02          /* Port 1 for input */
#define PORT1_OUT       0x00          /* Port 2 for output */

/* Group 1 mode commands */

#define MODE1N2_0       0x80          /* Mode 0 for group 1 */
#define MODE1N2_1       0x84          /* Mode 1 for group 1 */

/* Group 0 direction commands */

#define PORT2_IN_MSB    0x08          /* MSB of port 2 for input */
#define PORT2_OUT_MSB   0x00          /* MSB of port 2 for output */
#define PORT0_IN        0x10          /* Port 0 for input */
#define PORT0_OUT       0x00          /* Port 0 for output */

/* Group 0 mode commands */

#define MODE0N2_0       0x80          /* Mode 0 for group 0 */
#define MODE0N2_1       0xA0          /* Mode 1 for group 0 */
#define MODE0N2_2       0xC0          /* Mode 2 for group 0 */

```

```

main()
{
unsigned mode_word;

    /* Example #1 : Init all 48 lines for input */

mode_word = MODE0N2_0 | MODE1N2_0 | PORT0_IN | PORT1_IN | PORT2_IN_MSB |
    PORT2_IN_LSB;
    outp(PIO1_CMD,mode_word); /* Init the first chip */
    outp(PIO2_CMD,mode_word); /* and then the second chip */

    /* Example #2 : Init PIO1 for
        PORT 0 = input
        PORT 1 = output
        PORT 2 LSB = input
        PORT 2 MSB = output

                Init PIO2 for

        PORT 0 = output
        PORT 1 = output
        PORT 2 LSB = output
        PORT 2 MSB = input
    */

mode_word = MODE0N2_0 | MODE1N2_0 | PORT0_IN | PORT1_OUT |
    PORT2_IN_LSB | PORT2_OUT_MSB;
    outp(PIO1_CMD,mode_word); /* Init the first chip as desired */

mode_word = MODE0N2_0 | MODE1N2_0 | PORT0_OUT | PORT1_OUT |
    PORT2_OUT_LSB | PORT2_IN_LSB;
    outp(PIO2_CMD,mode_word); /* Init the second chip */

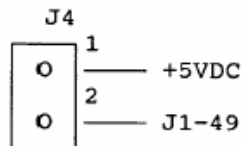
}

```

FIGURE 2-1
J2 I/O PIN-OUT

DEVICE #	PPI #	CONNECTOR	PIN #	8255/82C55 FUNCTION
U1	0	J2	1	PA0
			3	PA1
			5	PA2
			7	PA3
			9	PA4
			11	PA5
			13	PA6
			15	PA7
			17	PB0
			19	PB1
			21	PB2
			23	PB3
			25	PB4
			27	PB5
			29	PB6
			31	PB7
			33	PC0
			35	PC1
			37	PC2
			39	PC3
			41	PC4
			43	PC5
			45	PC6
			47	PC7
			49	J4 + 5VDC JUMPER

NOTE: All even numbered pins on J2 are ground.

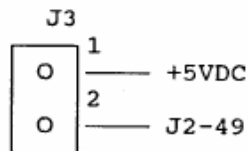


NOTE: Installing a jumper on J4 will connect +5 VDC to J2-49.

FIGURE 2-2
J1 I/O PIN-OUT

DEVICE #	PPI #	CONNECTOR	PIN #	8255/82C55 FUNCTION
U4	1	J1	1	PA0
			3	PA1
			5	PA2
			7	PA3
			9	PA4
			11	PA5
			13	PA6
			15	PA7
			17	PB0
			19	PB1
			21	PB2
			23	PB3
			25	PB4
			27	PB5
			29	PB6
			31	PB7
			33	PC0
			35	PC1
			37	PC2
			39	PC3
			41	PC4
			43	PC5
			45	PC6
			47	PC7
			49	J3 + 5VDC JUMPER

NOTE: All even numbered pins on J1 are ground.



NOTE: Installing a jumper on J3 will connect +5 VDC to J1-49.

APPENDIX

Intel 82C55A CMOS PROGRAMMABLE PERIPHERAL INTERFACE

Reprint datasheet	Intel_82C55A.pdf
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Cable Drawings

Part Number	Description
CBL-115-4	4 ft., 50 conductor ribbon cable with edge connector on one end
CBL-129-4	4 ft., 50 conductor ribbon cable with 50-pin 0.10" sockets on both ends

Software Examples

Initialization routine for 82C55 (Assembly Language)	8255INIT.ZIP
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3. Invoice number and date of purchase (if available), and original purchase order number.
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