

OPERATIONS MANUAL

PCM-UIO96B

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REVISION HISTORY

P/N 403-0285-000

ECO NUMBER	DATE CODE	REVISION
ORIGINATED	990818	A
99-95	991104	A1
02-76	021203	A2
03-31	030410	A3
07-36	070319	A4
10-82	111208	A5

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1 GENERAL INFORMATION

1.1 FEATURES

- 96 Digital I/O Lines
- PC/104 16-bit Interface
- Each line can serve as an input or an output
- Readback capability on all output lines
- Programmable polarity event sense on 48 lines
- Compatible with standard I/O racks
- +5 Volt only operation
- Extended temperature range -40°C to +85°C

1.2 GENERAL DESCRIPTION

The PCM-UIO96B is a highly versatile PC/104 module providing 96 lines of digital I/O. It is unique in its ability to monitor 48 lines for both rising and falling digital edge transitions, latch them, and then issue an interrupt to the host processor. The application interrupt service routine can quickly determine, through a series of interrupt identification registers, the exact port(s) and bit(s) which have transitioned. The PCM-UIO96B utilizes the WinSystems' WS16C48 ASIC High Density I/O Chip (HDIO). The first 48 lines are capable of fully latched event sensing with the sense polarity being software programmable. Four 50-pin I/O connectors allow for easy mating with industry standard I/O racks.

1.3 SPECIFICATIONS

1.3.1 Electrical

Bus Interface:	PC/104 16-Bit
VCC:	+5V +/-5% @ 24mA typical with no I/O connections
I/O Addressing:	12-bit user jumperable base address. Each board uses 32 consecutive addresses

1.3.2 Mechanical

Dimensions:	3.6" x 3.8"
PC Board:	FR-4 Epoxy glass with 2 signal layers, 2 power planes, screened component legend and plated through holes.
Jumpers:	0.025" square posts on 0.100" centers
Connectors:	50 Pin 0.10" grid RN type IDH-50-LP

1.3.3 Environmental

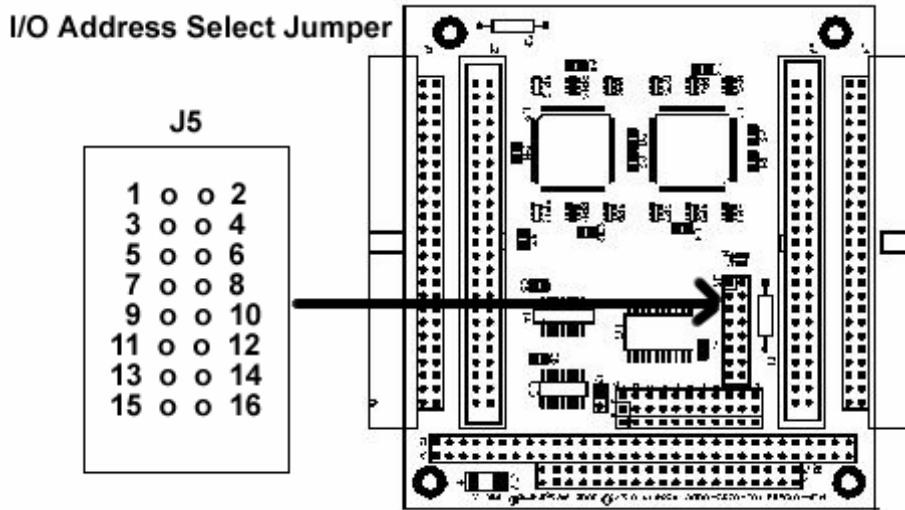
Operating Temperature:	-40°C to +85°C
Non Condensing Humidity:	5% to 95%

2 PCM-UIO96B TECHNICAL REFERENCE

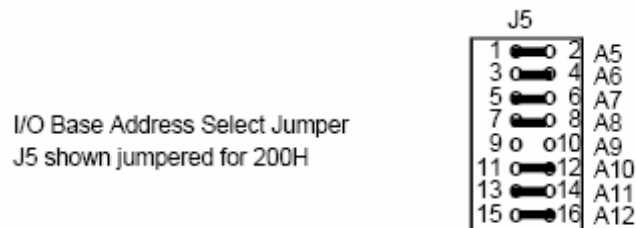
2.1 INTRODUCTION

This section of the manual is intended to provide the necessary information regarding configuration and usage of the PCM-UIO96B. WinSystems maintains a Technical Support Group to help answer questions regarding configuration, usage, or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time.

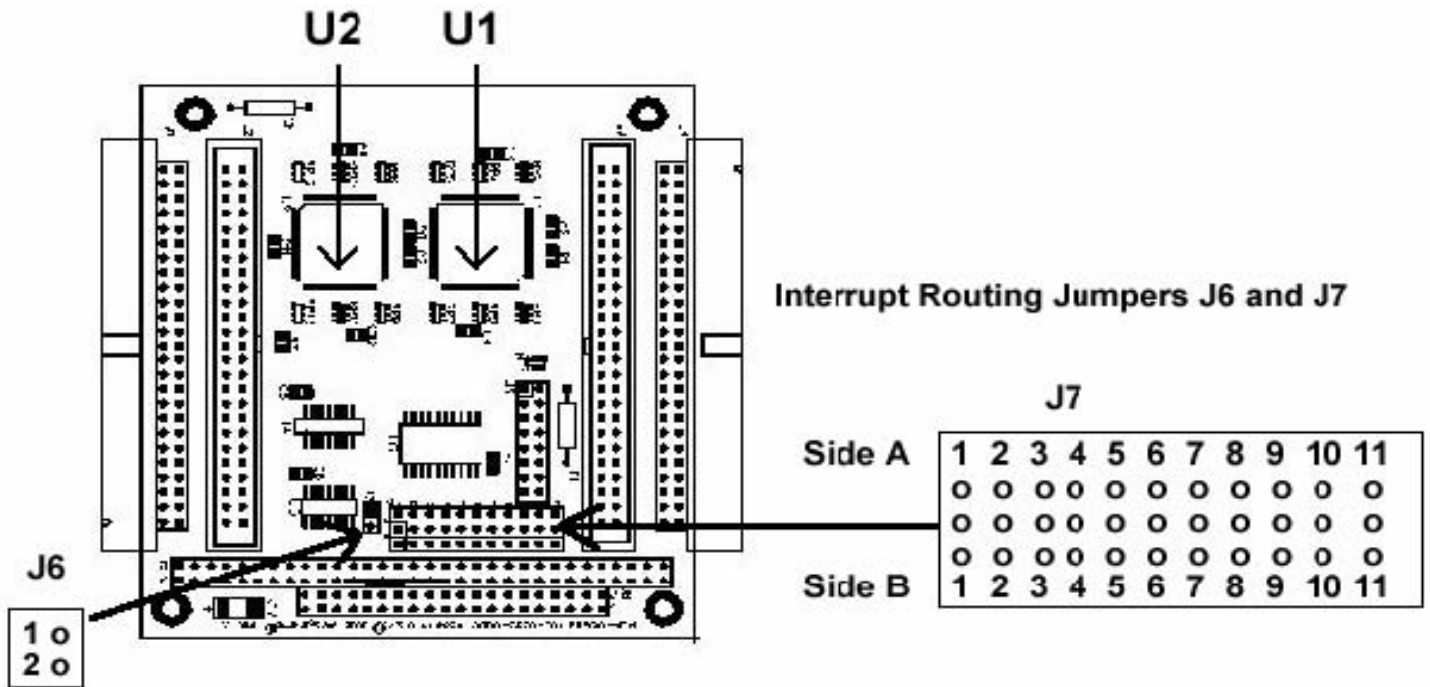
2.2 I/O ADDRESS SELECTION



The PCM-UIO96B requires 32 consecutive I/O addresses beginning on a 32 byte boundary. The jumper block at J5 allows for user selection of the base address. Address selection is made by placing a jumper on the jumper pair for the address bit if a '0' is desired or leaving the address bit open if a '1' is required for the desired address. U2 is located at the Base Address, U1 is located at the Base Address plus 10 Hex. The illustration below shows the relationship between the address bit and the jumper positions and a sample jumpering for a base address of 200H.

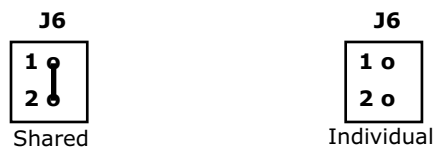


2.3 INTERRUPT ROUTING SELECTION



2.3.1 Shared Interrupts

For shared interrupts on the PC/104 bus, J6 must be jumpered pins 1-2. For individual interrupts, J6 should remain unjumpered as shown below.



2.3.2 Interrupt Selection

When desired, the PCM-UIO96B can generate an interrupt on up to 48 different lines each with its own polarity select. This interrupt can be routed to the PC/104 bus via the jumper at J7. J7 is a three row eleven pin interrupt routing block, side A directs interrupts to connector J1, side B directs interrupts to connector J4, and the center row connects directly to the PC/104 bus interrupt inputs.

