

OPERATIONS MANUAL SAT-520PLUS

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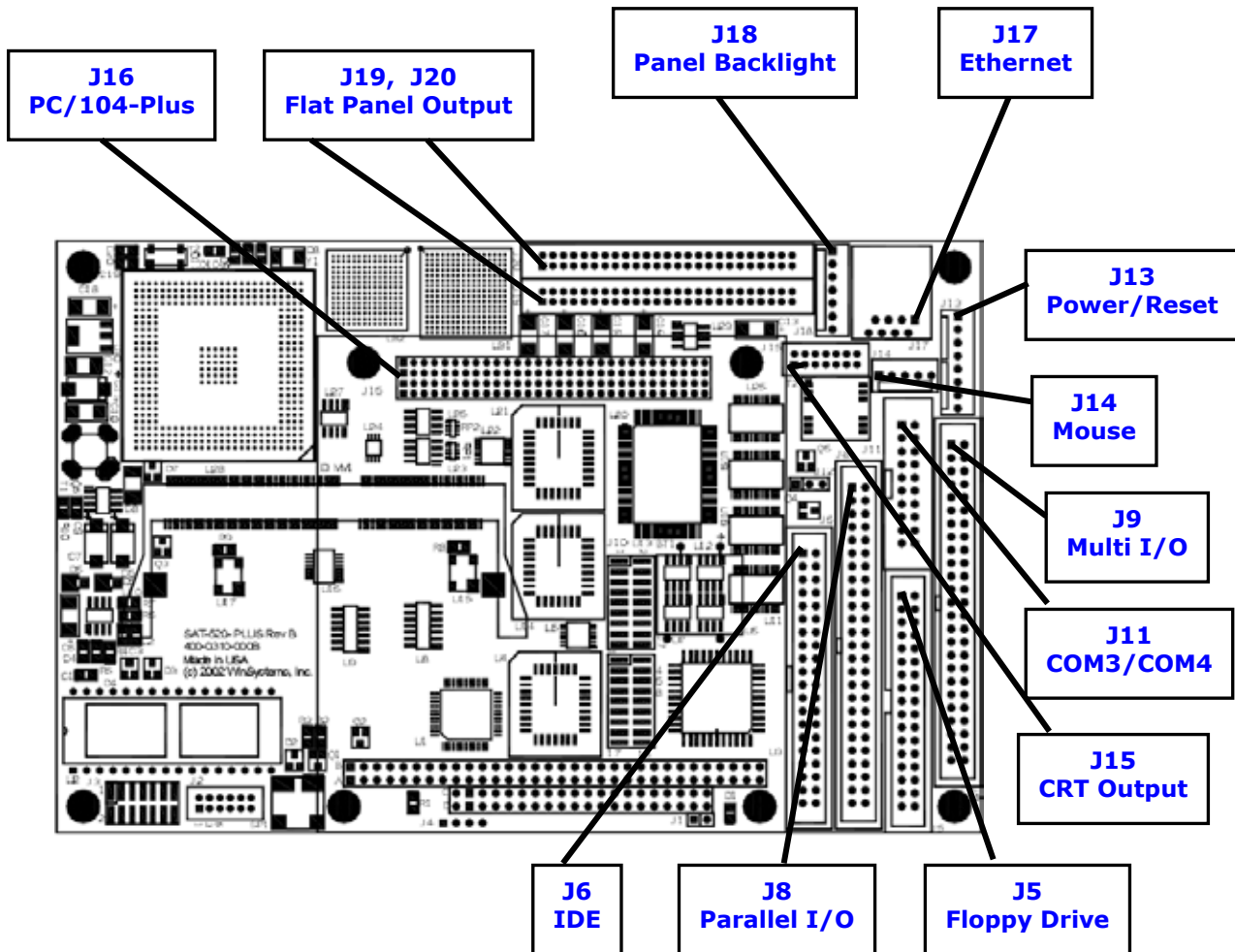
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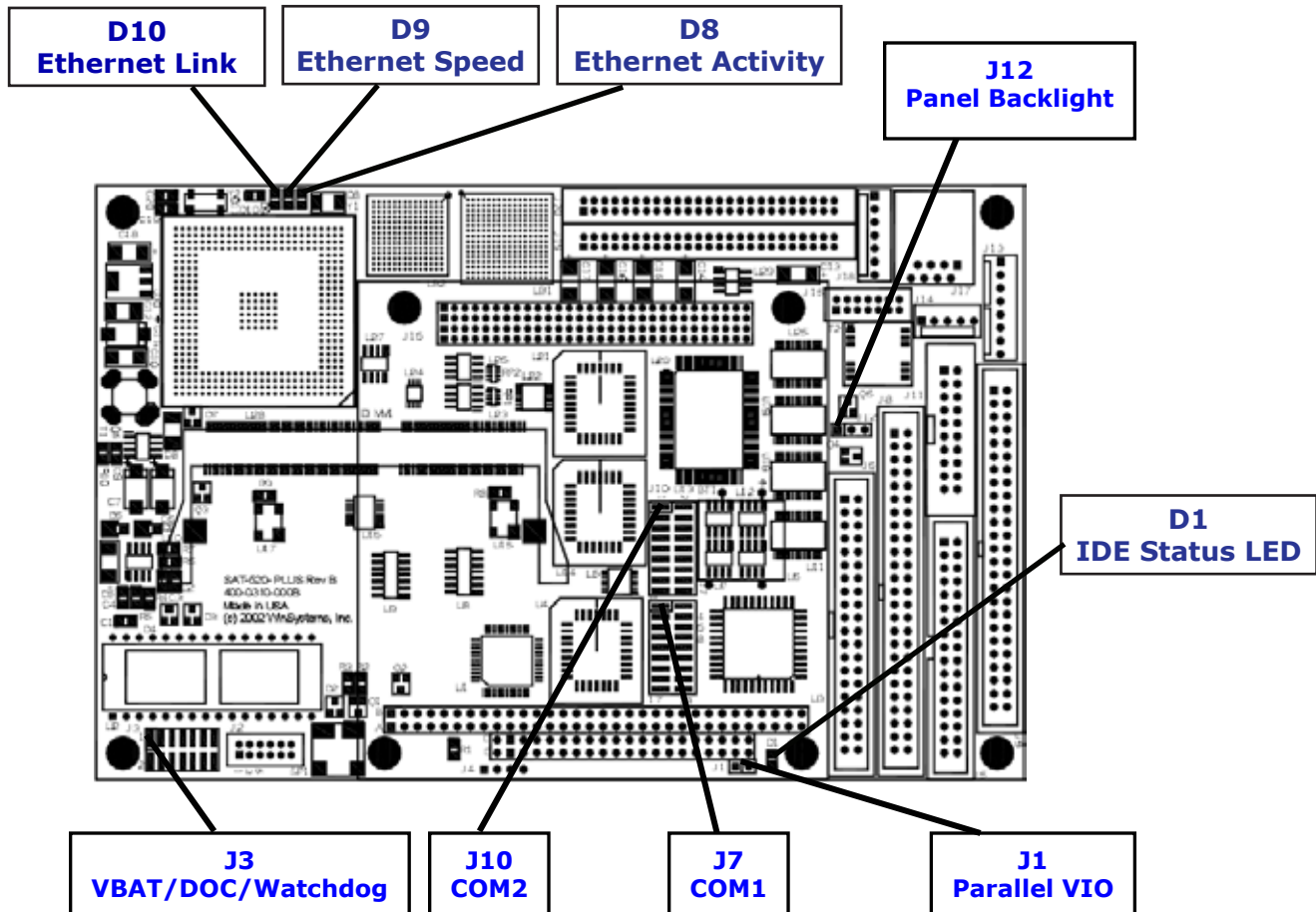
For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



Visual Index – Quick Reference

Top View - Jumpers & LEDs

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



Introduction

This manual is intended to provide the necessary information regarding configuration and usage of the SAT-520PLUS board. WinSystems maintains a Technical Support Group to help answer questions regarding usage, or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time.

General Information

Features

- AMD Elan SC520 Chipset/Processor
- 5x86 Processor at 133MHz
- 16KB Write Back Cache
- On Chip Floating Point Coprocessor
- User Upgradeable SODIMM SDRAM Memory
- Solid State Disk (DiskOnChip[®]) support
- Intel 82551ER 10/100 Ethernet Port
- 4 RS-232 Serial Ports with 16 byte FIFO's
- PS/2 Keyboard and Mouse support
- 32-bit PC/104Plus Expansion Bus
- 16-bit PC/104 Expansion Bus
- Single 5 Volt supply requirement
- Industry Standard Phoenix BIOS in user upgradeable Flash
- SPP/EPP/ECP PnP Parallel printer port
- Standard PC-AT architecture runs DOS, Windows, Linux, and other PC software
- 24 general purpose TTL digital I/O lines (82C55A)
- High-resolution CRT and flat panel controller with hardware Windows accelerator
- 24 Digital I/O lines
- -40°C to +85°C operation
- BIOS Extension socket

General Description

The SAT-520Plus is a highly integrated PC/104 and PC/104Plus expandable module with x86 compatibility and standard PC-AT architecture. It utilizes the latest of AMD's embedded processors, the ELAN SC520. The SC520 incorporates a 5x86 CPU core running at 133MHz along with a full 33MHz PCI host bridge, internal AT style peripherals, dual serial ports, and an IDE interface. The addition of the SMSC 37B727 adds the keyboard/mouse controller, two more plug-n-play serial ports, and a SPP/EPP/ECP parallel printer port, dual floppy disk interface. 24 lines of digital I/O, VGA and flat panel support also adds to the expansive feature set. Also onboard the SAT-520Plus is the popular Intel 82551ER10/100 Ethernet controller making this board an excellent choice for embedded applications requiring integrated networking. The 133MHz 5x86 CPU core and the integrated floating point processor offer an excellent compromise between computing power and power consumption. Feature expansion is also supported via either the popular PC/104 expansion bus or through the newer high-performance PCI type PC/104Plus expansion bus. The SAT-520Plus supports both standard rotational media drives, floppy and hard disk, or the popular DiskOnChip[®] flash modules in sizes ranging from 8 to 288 Mbytes.

SAT-520Plus Technical Reference

The SAT-520Plus uses the latest AMD embedded processor/chipset solution, the Elan SC520. The SC520 contains the following subsystems:

- 133MHz Am5X86 CPU core with floating point unit and a 16KB write-back cache
- Integrated PCI 2.2 compliant host bridge running at 33MHz
- SDRAM Controller
- ROM/Flash Controller
- Programmable Interval Timers
- Real Time clock/CMOS RAM
- Programmable Interrupt Controllers
- Programmable DMA Controllers
- Dual 16550 Compatible Serial Ports
- Dual IDE Chip Selects
- PS/2 Style Gate A20 and reset functions

The SAT-520Plus augments the inherent feature set of the AMD SC520 by adding the SMSC 37C727 PnP Super I/O chip. This chip contains these subsystems.

- Dual Floppy disk interface
- PS/2 Mouse controller
- PS/2 Keyboard controller
- Two 16550 compatible serial ports
- SPP/EPP/ECP compatible parallel printer port

The SAT-520Plus included a fourth generation CRT/Flat panel controller that supports standard VGA output as well as a variety of Flat Panel Displays.

The SAT-520Plus also includes an 82C55A-type device supporting 24 lines of digital I/O.

The SAT-520Plus also utilizes the Intel 82551ER10/100 Ethernet Controller for compatibility with a variety of network operating systems and software.

Support for the M-Systems DiskOnChip[®] device is present which allows for Flash drives in sizes from 8 to 288 MB.

AMD Elan SC520 Processor – The AMD SC520 is the latest in AMD's line of embedded processors. The SC520 incorporates the CPU, FPU, DRAM controller, Flash/ROM controller, PCI controller, RTC/CMOS RAM, and Chip selections for DOC support and the IDE interface.

The processor is supplied from AMD in a 388-pin PBGA package and is soldered directly to the board at the factory. This part is not user replaceable or upgradeable. The core CPU runs at a base clock frequency of 33MHz. An internal software controlled multiplier of either 3X or 4X results in internal processor speeds of either 100MHz or 133MHz. The multiplier selection is user definable using the [Phoenix BIOS Setup](#) utility.

Memory Selection and Installation – The SAT-520Plus comes from the factory with 0MB of RAM. RAM memory must be installed by the user and must meet the following criteria:

32, 64, 128 or 256MB 144-Pin SODIMM SDRAM, PC66 or PC100 minimum, with gold fingers

WinSystems qualified SODIMMs are available from Crucial Technologies or online through the WinSystems web site at www.winsystems.com or directly from WinSystems. WinSystems cannot warrant the operation of systems using non-qualified SODIMM modules.

Installation is accomplished by inserting the module into the connector on the front of the board at approximately a 30-degree angle. Press firmly to fully seat the module into the connector and then press the module downward to snap it into the retaining clamps.

Removal is accomplished by gently pulling outward on the retaining clamps until the module springs up to the appropriate removal angle.

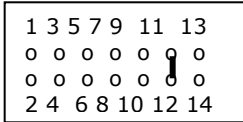
Power/Reset Connection – Power is supplied to the SAT-520Plus through the 8-pin Molex connector at **J13**. The pin definitions are:



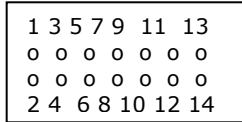
1 o	-12V
2 o	+12V
3 o	+5V
4 o	+5V
5 o	GND
6 o	GND
7 o	GND
8 o	RESET*

An optional momentary-contact, normally-open reset button can be connected between pin 8 and ground.

BIOS Extension Socket – The SAT-520Plus supports the use of the Atmel 27C070 EPROM, or the Atmel 29C010 EEPROM to be used as an extended BIOS for the user. Code for these parts must be offset 2000Hex bytes from the start of the prom. The 32-pin socket at U4 is used to contain the Atmel devices used for the BIOS. The BIOS is memory mapped into a 8Kbyte hole at segment D2000. An example jumpering for **J3** with write enabled and disabled is shown below.



Extension write enabled



Extension write disabled

NOTE: The write enable/disable functions apply only to the Atmel 29C010 part.

Floppy Disk Interface – The SAT-520Plus and the Phoenix BIOS support up to two 5¼" or 3½" floppy disk drives. The drive types are configured using the BIOS setup menus. The drives are connected via the I/O connector at **J5**. Note that the interconnect cable to the drives is a standard floppy I/O cable used on desktop PC's. The cable must have the twisted section prior to the drive A position. The pin definitions for the **J5** connector are:



GND	1 o o 2	RPM/LC
GND	3 o o 4	N/C
GND	5 o o 6	N/C
GND	7 o o 8	INDEX
GND	9 o o 10	MTR0
GND	11 o o 12	DRV1
GND	13 o o 14	DRV0
GND	15 o o 16	MTR1
GND	17 o o 18	DIR
GND	19 o o 20	STEP
GND	21 o o 22	WDATA
GND	23 o o 24	WGATE
GND	25 o o 26	TRK0
GND	27 o o 28	WPRT
GND	29 o o 30	RDATA
GND	31 o o 32	HDSEL
GND	33 o o 34	DSKCHG

IDE Interface – The SAT-520Plus supports up to two IDE devices. Connection to IDE hard disks and CD-ROMs is most easily accomplished when using the WinSystems adapter cable, part number CBL-126-9, connected to **J6**. This cable allows for the attachment of one standard 40-pin IDE device. Configuration of any IDE device is accomplished using the Phoenix BIOS setup menus.



The pin definitions for the 40-pin IDE connector are:

RESET	1 0 0 2	GND
D7	3 0 0 4	D8
D6	5 0 0 6	D9D
D5	7 0 0 8	10
D4	9 0 0 10	C11
D3	11 0 0 12	D12
D2	13 0 0 14	D13
D1	15 0 0 16	D14
D0	17 0 0 18	D15
GND	19 0 0 20	N/C
GND	21 0 0 22	GND
IOW	23 0 0 24	GND
IOR	25 0 0 26	GND
N/C	27 0 0 28	ALE
N/C	29 0 0 30	GND
INTRQ	31 0 0 32	IOCS16
A1	33 0 0 34	N/C
A0	35 0 0 36	A2
HDCS0	37 0 0 38	HDCS1
N/C	39 0 0 40	GND

An IDE Status LED, **D1**, provides visual status during IDE data transfer.

DiskOnChip Configuration – The SAT-520Plus supports solid state disks using the M-Systems DiskOnChip (DOC) flash devices (www.m-sys.com). These devices are available in sizes ranging from 8Mbytes to the currently available maximum size of 288Mbytes. These devices are inherently supported by the VIOS and DOS (they appear as hard disk to DOS) and are supported by a variety of other operating systems. Current non DOS driver support is available directly from the M-Systems website.

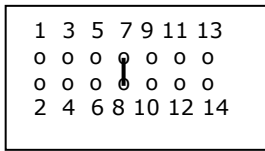
The DOC device is ordinarily used in systems without an actual hard disk. In these cases the hard drive settings for both the C: and D: drives should be set to NONE in the CMOS Setup Menus. The DOC will then appear as drive C: and standard partitioning and formatting software may be used to prepare it to boot. The boot-up time may be dramatically improved by disabling the SC520 IDE controllers in the CMOS setup when an actual hard disk will not be connected.

When the DOC is used in conjunction with an actual hard disk it automatically becomes the secondary of D: drive. This can be useful when it is desired to load a DOC with a large number of files that may currently reside on the hard disk. This characteristic of becoming a secondary drive to an actual hard disk is referred to by M-Systems as "Last Drive". This characteristic may be altered such that the DOC will become the primary drive (or First Drive) by using the *DFORMAT* utility available from M-Systems. In this case it is possible to boot from the DOC and access the hard disk as the D: drive. Refer to the utilities documentation accompanying the download from M-Systems for more information if this mode is required.

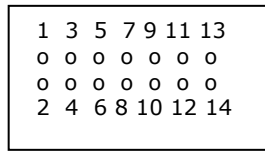
The DOC device is installed in the socket-strips designated as U2. Pin 1 of the DOC should be oriented toward the outer edge of the board.



The DOC is enabled and disabled by using pins 7 and 8 of the jumper block at **J3**. The jumpering configurations for **J3** are:



DOC Enabled



DOC Disabled

Serial Interface – The SAT-520Plus contains four 16550 compatible serial ports. COM3 and COM4 are RS-232 only and are present inside the SMSC 37C727 Super I/O chip. COM3 and COM4 are fully plug-and-play compatible (PnP) and are configurable using the BIOS setup menus. Connection to COM3 and COM4 is made via the connector at **J11**. **J11** pinout is shown on the following page.



COM1 and COM2 can be individually configured for any one of a number of operating modes using the jumper blocks at J7 and **J10**. These modes include:

1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Modes 2, 4 and 5 require the RTS bit in the MCR (Bit 1) be set in order to Transmit.
Modes 4 and 6 require that RTS in the MCR (Bit 1) be deasserted in order to receive.

Each of the RS-422/RS-485 modes also allows for jumper selection of transmit and/or receive termination resistor(s). There is an 18-pin configuration jumper for both COM1 and COM2 ports that allow the user to select the operating mode and its optional features and termination. The jumper numbers and corresponding port numbers are shown in the following table. There are three choices for termination when RS-422 or RS-485 modes are used.

- TX(100) - Places a 100 ohm resistor across the TX+/TX- pair.
- RX(100) - Places a 100 ohm resistor across the RX+/RX- pair.
- TX-RX(300) - Places a 100 ohm resistor from +5V to TX/RX+, a 100 ohm resistor from TX-RX- to ground and a 100 ohm resistor between TX-RX+ and TX/RX-.

Each channel is configured using **J7** or **J10** as shown above. The table below shows the appropriate jumpering for **J7** and **J10** in the various modes.

Mode #	Description	Jumpers	Termination		
			TX (100)	RX (100)	TX/RX (300)
1	RS-232	1-2	N/A	N/A	N/A
2	RS-422 RTS Enable	3-4, 9-10	11-12	17-18	11-12 13-14 15-16
3	RS-422 Auto Enable	3-5, 9-10 (One node must use TX/RX 300 Termination)	N/A	17-18	11-12 13-14 15-16
4	RS-485 RTS Enable	3-4, 7-8	11-12	N/A	11-12 13-14 15-16
5	RS-485 RTS Enable with Echo-Back	3-4, 8-6	11-12	N/A	11-12 13-14 15-16
6	RS-485 Auto Enable	3-5, 7-8 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16
7	RS-485 Auto Enable with Echo-Back	3-5, 8-6 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16

Serial Port I/O Definitions – Serial port definitions for all four COM ports are the same when used in their various modes. Pin definitions for each are shown below in each possible mode.



DB9 Male	RS-232 Mode	RS-422 Mode	RS-485 Mode
1 2 3 4 5 0 0 0 0 0 0 0 0 0 6 7 8 9	1. DCD 2. RX 3. TX 4. DTR 5. GND 6. DSR 7. RTS 8. CTS 9. RI	1. N/A 2. TX+ 3. TX+ 4. N/A 5. GND 6. RX+ 7. RX- 8. N/A 9. N/A	1. N/A 2. TX/RX+ 3. TX/RX- 4. N/A 5. GND 6. N/A 7. N/A 8. N/A 9. N/A

COM3 and COM4 are RS-232 only and are terminated at **J11**. An adapter cable is available from WinSystems, part number CBL-173-1, adapting **J11** to two standard DB9M connectors. The pin definitions for **J11** are:

COM3 – DCD	1 0 0 2	COM3 – DSR
COM3 – RX	3 0 0 4	COM3 – RTS
COM3 – TX	5 0 0 6	COM3 – CTS
COM3 – DTR	7 0 0 8	COM3 – RI
GND	9 0 0 10	N/C
COM4 – DCD	11 0 0 12	COM4 – DSR
COM4 – RX	13 0 0 14	COM4 – RTS
COM4 – TX	15 0 0 16	COM4 – CTS
COM4 – DTR	17 0 0 18	COM4 – RI
GND	19 0 0 20	N/C

Ethernet Controller – One of the principal features of the SAT-520Plus is the inclusion of the 10/100 Ethernet controller. The popular Intel 82551ER high-integration NIC supports both IEEE 802.3 10BASE-T and 100BASE-TX in a fully auto-negotiating mode. The 82551 ER integrates both the Media Access Controller (MAC) and the physical layer (PHY) on a single chip. The 82551ER is a full bus mastering PCI controller and also incorporates 6K of buffer memory. Full duplex operation provides throughput of up to 200Mbps of fast Ethernet segments.

Intel provides a vast array of driver support for all of the popular network operating systems including: Windows CE, Windows 95, Windows 98SE, Windows ME, Windows NT, Windows 2000, Novell Netware 3.11-4.1, Solaris, Linux, and Unix.

The Ethernet section of the SAT-520Plus is a full PCO PnP (plug-and-play) implementation coupled with the Phoenix PCI BIOS which assigns the necessary I/O, Memory, DMA, and IRQ resources required by the controller. Connection to the network is made via the RJ-45 connector at **J17**. There are three Ethernet status LEDs on the edge of the board. The purpose of each LED is:

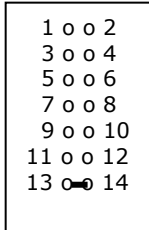
D10	(YELLOW)	LINK ACTIVE
D9	(RED)	SPEED INDICATION – LIT=100BASE-TX
D8	(GREEN)	ACTIVITY

NOTE: WinSystems cannot provide technical support for direct programming of the 82551ER controller. We suggest utilizing a TCP/IP stack of Network O/S that allows the use of preexisting 82551 drivers.

Ethernet Drivers – The 82551ER is supported by a number of operating systems directly. Intel provides the latest drivers through their web site at: <http://developer.intel.com/design/network/drivers/>

Alternately, most drivers will be available for the WinSystems site at: <http://www.winsystems.com>

Parallel I/O – The SAT-520Plus contains an 82C55A type device supporting 24 lines of digital I/O. These 24 lines are terminated at J8, and are enabled and disabled using pins 13 and 14 of **J3**. When **J3** pins 13 and 14 are jumpered, digital I/O is enabled. An example is shown below. The base address of the 82C55A is 1E8H. For programming information, refer to the [Intel 82C55A Datasheet](#).



Parallel I/O enabled

Parallel I/O Connector – The parallel I/O connector is located at **J8**. The pin definitions are:



PORT C BIT 7	1 0 0 2	GND
PORT C BIT 6	3 0 0 4	GND
PORT C BIT 5	5 0 0 6	GND
PORT C BIT 4	7 0 0 8	GND
PORT C BIT 3	9 0 0 10	GND
PORT C BIT 2	11 0 0 12	GND
PORT C BIT 1	13 0 0 14	GND
PORT C BIT 0	15 0 0 16	GND
PORT B BIT 7	17 0 0 18	GND
PORT B BIT 6	19 0 0 20	GND
PORT B BIT 5	21 0 0 22	GND
PORT B BIT 4	23 0 0 24	GND
PORT B BIT 3	25 0 0 26	GND
PORT B BIT 2	27 0 0 28	GND
PORT B BIT 1	29 0 0 30	GND
PORT B BIT 0	31 0 0 32	GND
PORT A BIT 7	33 0 0 34	GND
PORT A BIT 6	35 0 0 36	GND
PORT A BIT 5	37 0 0 38	GND
PORT A BIT 4	39 0 0 40	GND
PORT A BIT 3	41 0 0 42	GND
PORT A BIT 2	43 0 0 44	GND
PORT A BIT 1	45 0 0 46	GND
PORT A BIT 0	47 0 0 48	GND
+5V	49 0 0 50	GND

NOTE: Pin 49 of J8 may be configured to supply +5 volts to pin 49 by placing a jumper on **J1**. The current draw from pin 49 should not exceed 300mA.



VGA Configuration – The SAT-520Plus uses a fourth generation CRT/Flat panel Super VGA controller. It supports standard VGA output as well as a variety of Flat Panel Displays using optional Flat Panel Adapter (FPA) kits. The video on the SAT-520Plus uses the Asilant 69000 series of high performance VGA controllers. The Asilant controller supports standard and Super-VGA as well as color and monochrome panels with 8, 9, 12, 15, 16, 18, 24 and 36-bit interfaces. WinSystems provides flat panel support through a series of Flat Panel kits. Contact your WinSystems' Applications Engineer for the most current list of available FPAs and supported panels.

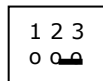


Details regarding interfacing to specific Flat Panels is not provided in this manual but should be referenced in the documentation accompanying the FPA kit. Attempted connection to any flat panel not directly supported by a WinSystems' FPA module is at the user's risk and extreme care should be exercised to avoid damaging or destroying the panel.



HAZARD WARNING: LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring or handling the inverter output. To avoid danger of shock and to avoid damaging fragile and expensive panels, make all connection changes with power removed.

NOTE: J12 must be jumpered 1-2 for Sharp type panels, and 2-3 for NEC type panels. An example jumpering for NEC panels is shown below.



Panel Backlight Enable

CRT Output Connection – Video output to a standard VGA monitor is made via the connector at **J15**. An adapter cable, part number CBL-234-1, is available from WinSystems to adapt from **J15** to the standard DB15 VGA connector. The pin definitions for the **J15** connector are:



RED	1 0 0 2	GND
GREEN	3 0 0 4	GND
BLUE	5 0 0 6	GND
HSYNC	7 0 0 8	GND
VSYNC	9 0 0 10	GND
DDCDATA	11 0 0 12	GND
DDCCLK	13 0 0 14	VCC

Panel Backlight Connection – Panel Backlight connection is made via the connector at **J18**. The pinout for **J18** is:



0 1	+12
0 2	+12
0 3	GND
0 4	GND
0 5	ENBKL
0 6	VCC
0 7	VCC

Flat Panel Output Connection – Connection to all flat panels is made via the two 50-pin connectors at **J19** and **J20**. These connectors are cabled to the appropriate FPA (Flat Panel Adapter) module which then breaks out the necessary cabling for attachment to the panel itself. The FPA module also supplies any special controls that may be needed for the panel. Refer to the FPA documentation for specific hook-up instructions. The pin definitions for **J19** and **J20** are:



J19		J20	
SW0	1 0 0 2	SW1	FP12
SW2	3 0 0 4	SW3	FP13
FP0	5 0 0 6	GND	FP14
FP1	7 0 0 8	GND	FP15
FP2	9 0 0 10	GND	FP16
FP3	11 0 0 12	GND	FP17
FP4	13 0 0 14	GND	FP18
FP5	15 0 0 16	GND	FP19
FP6	17 0 0 18	GND	FP20
FP7	19 0 0 20	GND	FP21
FP8	21 0 0 22	GND	FP22
FP9	23 0 0 24	GND	FP23
FP10	25 0 0 26	GND	FP24
FP11	27 0 0 28	GND	FP25
PCSHCLK	29 0 0 30	GND	FP26
PCFLM	31 0 0 32	GND	FP27
PCLP	33 0 0 34	GND	FP28
PCM	35 0 0 36	GND	FP29
PHSYNC	37 0 0 38	GND	FP30
PVSYNC	39 0 0 40	GND	FP31
ENVCC	41 0 0 42	GND	FP32
ENBKL	43 0 0 44	GND	FP33
ENVEE	45 0 0 46	-12V	FP34
+12V	47 0 0 48	+12V	FP35
SWVCC	49 0 0 50	SWVCC	SWVCC

Parallel Printer Port – The SAT-520Plus supports a parallel printer port contained in the SMSC37C727 super I/O chip and is terminated at the Multi-I/O connector at **J9**. This port is fully PnP compatible and is configurable using the Phoenix BIOS setup menus. The parallel port can be configured for SPP, EPP and ECP modes. The pin definitions for the DB25 connector using the CBL-247-1 are:



STROBE	1 0 0 14	AUTOFD
PD0	2 0 0 15	ERROR
PD1	3 0 0 16	INIT
PD2	4 0 0 17	SLIN
PD3	5 0 0 18	GND
PD4	6 0 0 19	GND
PD5	7 0 0 20	GND
PD6	8 0 0 21	GND
PD7	9 0 0 22	GND
ACK	10 0 0 23	GND
BUSY	11 0 0 24	GND
PE	12 0 0 25	GND
SLCT	13 0	

Keyboard Interface – The SAT-520Plus contains onboard PS/2 style keyboard controller. Connection is made through the Multi-I/O cable connection at **J9**. An adapter cable, CBL-247-1 is available from WinSystems to make ready access to all of the devices terminated at the Multi-I/O connector. Users who may wish to construct their own cables should refer to the Multi-I/O connector pin definitions given later in this manual.

Multi-I/O Connector – The I/O to the primary serial channels, the printer port, and keyboard are all terminated via the connector at **J9**. WinSystems’ multi-I/O cable, part number CBL-247-1, is available to adapt to the conventional I/O connectors. The pin definitions for **J9** are shown here:



COM1 - DCD	1 0 0 2	COM1 - DSR
COM1 - RXD	3 0 0 4	COM1 - RTS
COM1 - TXD	5 0 0 6	COM1 - CTC
COM1 - DTR	7 0 0 8	COM1 - RI
COM1 - GND	9 0 0 10	COM2 - DCD
COM2 - DSR	11 0 0 12	COM2 - RSX
COM2 - RTS	13 0 0 14	COM2 - TXD
COM2 - CTC	15 0 0 16	COM2 - DTR
COM2 - RI	17 0 0 18	COM2 - GND
LPT - STROBE	19 0 0 20	LPT - AUTOFD
LPT - PD0	21 0 0 22	LPT - ERROR
LPT - PD1	23 0 0 24	LPT - INIT
LPT - PD2	25 0 0 26	LPT - SLCTIN
LPT - PD3	27 0 0 28	LPT - GND
LPT - PD4	29 0 0 30	LPT - GND
LPT - PD5	31 0 0 32	LPT - GND
LPT - PD6	33 0 0 34	LPT - GND
LPT - PD7	35 0 0 36	LPT - GND
LPT - ACK	37 0 0 38	LPT - GND
LPT - BZY	39 0 0 40	LPT - GND
LPT - PE	41 0 0 42	LPT - GND
LPT - SLCT	43 0 0 44	KEYBD - GND
KEYBD - GND	45 0 0 46	KEYBD - GND
KEYBD - KDATA	47 0 0 48	KEYBD - CLK
KEYBD - +5V	49 0 0 50	KEYBD - +5V

Mouse Interface – Connection to a mouse is made via the connector at **J14**. An adapter cable, CBL-225-1, is available from WinSystems to adapt to a conventional PS/2 mouse connector. The pinout for **J14** is:



1 0	MSDATA
2 0	N/C
3 0	GND
4 0	VCC
5 0	MSCLK

Real-Time Clock/Calendar and CMOS Setup RAM

The onboard 350mAH lithium battery provides power to the real-time clock and the CMOS setup RAM when power is removed. If it ever becomes necessary to have the CMOS RAM settings return to their default factory settings, with power off, reposition the **J3** jumper from pins 1-2 to pins 2-4 for approximately 30 seconds and then return the jumper to pins 1-2. At the next power-up the BIOS will load the factory defaults.



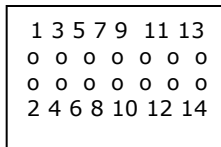
Watchdog Timer Configuration

The SAT-520Plus features a power-on voltage detect and a power-down/power brownout circuit to protect memory and I/O from faulty CPU operation during periods of illegal voltage levels. This supervisory circuit also features a watchdog timer which can be used to guard against software lockups. An internal self-timer with a period of 1/5 second will, when enabled, reset the CPU if the watchdog has not been serviced (petted) within the allotted time. There are three watchdog operational modes available on the SAT-520Plus. With a jumper placed on pins 5-6 of **J3**, the watchdog circuit is totally disabled and can never reset the processor. When **J3** pins are not jumpered, the watchdog timer is permanently enabled and timing begins immediately at power up. This mode is NOT compatible with the Phoenix BIOS or with MS-DOS but is available for directly embedded code that replaces the BIOS. The watchdog must be accessed at least every 1.5 seconds or a reset will occur. Petting in this mode is accomplished with a single I/O write (value ignored) to address 1EFH.



The alternate mode of operation is via software control to enable or disable the watchdog's operation. This mode is set by jumpering **J3** pins 3-5. In this mode the watchdog powers-up disabled and must be enabled in software before timing will begin. Enabling the watchdog is accomplished by writing a 1 to I/O port 1EEH. Writing a 0 to I/O address 1EEH will disable the watchdog. Once the watchdog is enabled, it must be serviced at least every 1.5 seconds or a rest will occur. Petting in this mode is accomplished with a single I/O write (value ignored) to address 1EFH.

J3 orientation



Status LED – An onboard LED can be used by software for signaling status or error conditions. The LED is illuminated by writing a 1 to I/O port 1EDH. The LED is turned off by writing a 0 to I/O address 1EDH.

Speaker/Sound Interface - An onboard audio transducer provides a high level audio output which is compatible with the standard PC speaker. This output is used by the BIOS to signal POST errors and may be used by user software for signaling purposes.

PC/104 Bus Interface – The SAT-520Plus supports the PC/104

bus which is basically the original ISA bus with the 16-bit extensions.

A vast array of PC/104 stack-on modules are available from WinSystems and other PC/104 suppliers. The PC/104 bus connector pin definitions are provided here for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.



GND	D0 ○ ○ C0	GND	IOCHK*	A1 ○ ○ B1	GND
MEMCS16*	D1 ○ ○ C1	SBHE*	SD7	A2 ○ ○ B2	RESET
IOCS16*	D2 ○ ○ C2	LA23	SD6	A3 ○ ○ B3	+5V
IRQ10	D3 ○ ○ C3	LA22	SD5	A4 ○ ○ B4	IRQ9
IRQ11	D4 ○ ○ C4	LA21	SD4	A5 ○ ○ B5	-5V
IRQ12	D5 ○ ○ C5	LA20	SD3	A6 ○ ○ B6	DRQ2
IRQ15	D6 ○ ○ C6	LA19	SD2	A7 ○ ○ B7	-12V
IRQ14	D7 ○ ○ C7	LA18	SD1	A8 ○ ○ B8	SRDY
DACK0*	D8 ○ ○ C8	LA17	SD0	A9 ○ ○ B9	+12V
DRQ0	D9 ○ ○ C9	MEMR*	IOCHRDY	A10 ○ ○ B10	KEY
DACK5*	D10 ○ ○ C10	MEMW*	AEN	A11 ○ ○ B11	SMEMW*
DRQ5	D11 ○ ○ C11	SD8	SA19	A12 ○ ○ B12	SMEMR*
DACK6*	D12 ○ ○ C12	SD9	SA18	A13 ○ ○ B13	IOW*
DRQ6	D13 ○ ○ C13	SD10	SA17	A14 ○ ○ B14	IOR*
DACK7*	D14 ○ ○ C14	SD11	SA16	A15 ○ ○ B15	DACK3*
DRQ7	D15 ○ ○ C15	SD12	SA15	A16 ○ ○ B16	DRQ3
+5V	D16 ○ ○ C16	SD13	SA14	A17 ○ ○ B17	DACK1*
MASTER*	D17 ○ ○ C17	SD14	SA13	A18 ○ ○ B18	DRQ1
GND	D18 ○ ○ C18	SD15	SA12	A19 ○ ○ B19	REFRESCH*
GND	D19 ○ ○ C19	KEY	SA11	A20 ○ ○ B20	BCLK
			SA10	A21 ○ ○ B21	IRQ7
			SA9	A22 ○ ○ B22	IRQ6
			SA8	A23 ○ ○ B23	IRQ5
			SA7	A24 ○ ○ B24	IRQ4
			SA6	A25 ○ ○ B25	IRQ3
			SA5	A26 ○ ○ B26	DACK2*
			SA4	A27 ○ ○ B27	T/C
			SA3	A28 ○ ○ B28	BALE
			SA2	A29 ○ ○ B29	+5V1
			SA1	A30 ○ ○ B30	OSC
			SA0	A31 ○ ○ B31	GND
			GND	A32 ○ ○ B32	GND

PC/104 Add-on Modules – The GP bus provided by the AMD Elan SC520 processor does a reasonably good job of implementing the ISA (PC/104) bus. There are, however, a few caveats and limitations that may not allow certain PC/104 add-on modules to function properly.

Pin Number	Pin Name	Caveat/Limitation
A1	IOCHK*	No bus level NMI support
B5	-5V	No support for -5 volts
B8	SRDY	There is no support for 0 wait state. All bus timing is fixed by the SC520
B19	Refresh/DACK0	No support for Refresh to the ISA bus
B20	BCLK	This is an asynchronous 8MHz clock
B30	OSC	This is an asynchronous 14.318MHz clock
D8	DACK0	No DMA channel 0 available
D9	DRQ0	No DMA channel 0 available
D12	DACK6	No support for DMA channel 6
D13	DRQ6	No support for DMA channel 6
D14	DACK7	No support for DMA channel 7
D15	DRQ7	No support for DMA channel 7
D17	MASTER	No support for alternate bus masters on the ISA bus

In addition to the table above, it must also be recognized that because of the large complement of I/O devices onboard. There may be few, if any, bus interrupts available to PC/104 add-on cards. In some cases turning off the onboard peripheral will free up the interrupt for use on the PC/104 bus.

The table below show the standard interrupt assignments and if they are available, and if the associated peripheral is disabled.

IRQ Number	Peripheral	Free when peripheral disabled
0	Heartbeat Tick	NO
1	Keyboard	NO
2	Slave PIC	YES
3	COM2	YES
4	COM1	N/A
5	Unassigned	NO
6	Floppy Controller	YES
7	Parallel Port	NO
8	RTC	YES
9	COM3	YES
10	PCI Routing	NO
11	COM4	YES
12	Mouse	NO
13	FPU	NO
14	Hard Disk	NO

IMPORTANT NOTE: Due to limitation with the Programmable Address Registers (PAR) within the SC520 processor, the I/O address range accessible via the PC/104 bus alters fairly significantly dependent upon the presence and type of video adapter installed. When a PC/104Plus video card is installed, I/O addresses below 200H are not accessible on the PC/104 Bus, therefore, all I/O cards must be mapped above 200H. This limitation does not exist when using a PC/104 video card, or when no video card is present.

PC-104-Plus Interface - The SAT-520Plus also supports peripheral expansion using the PC/104-Plus connector at **J16**. Up to three PC/104-Plus modules may be stacked onto the SAT-520Plus.



The onboard Ethernet is attached to Slot 4 and PC/104-Plus modules should be attached and configured beginning at Slot 1. The PC/104-Plus bus pin definitions are shown here for reference purposes only. Refer to the PC/104-Plus Bus Specification for signal definitions, timing and mechanical details.

Pin	A	B	C	D
1	GND/5.0 Key	RESERVED	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD06
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE3*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RTS*
29	+12V	INTA*	INTB*	INTC*
30	-12V	RESERVED	RESERVED	GND/3.3V KEY

Phoenix BIOS Setup

General Information – The SAT-520Plus comes equipped with a standard Phoenix Bios to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery-backed CMOS RAM within the clock/calendar. Access to this setup information is via the Setup utility in the Phoenix BIOS.

Entering Setup – To enter setup, power up the computer and press F2 when either the splash screen is displayed (when enabled) or when the “Press F2 for Setup” message is displayed.

Alternately, under certain error conditions a message similar to, “**Press F1 to Continue or F2 for Setup**” may be displayed. Press the desired key for the appropriate action. The BIOS will display the message, “**Entering Setup**” and will continue with the remainder of the POST routines. It may take a number of seconds before the main setup menu screen is displayed.

Setup Main Menu – Each of the available options on the main menu screen, illustrated here, will be discussed in this section.

PhoenixBIOS Setup Utility	
Main Advanced Boot Exit	
System Time : 11:34:27	Item Specific Help
System Date : 08/21/2002	
Legacy Diskette A: [1.44/1.2MB ½"]	<Tab>, <Shift-Tab>, or <Enter> selects field.
Legacy Diskette B: [Disabled]	
Primary Master [None]	
Primary Slave [None]	
System Memory : 640KB	
Extended Memory 63MB	
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults ESC Exit O Select Menu Enter Select Sub-Menu F10 Save and Exit	

Use the “**UP**” and “**DOWN**” arrow keys to move among the sections. Use the “**LEFT**” and “**RIGHT**” arrow keys to move to another menu page. Hit “+” or “-” to scroll through the selections, or hit “**ENTER**” when a selection is highlighted to enter a sub-menu or to see a list of choices.

System Time: This option allows for the setting of the time in the clock/calendar. “**ENTER**” is used to move from hours, to minutes, to seconds while the “+/-” keys adjust the value.

System Date: This option allows for setting the calendar to the current month, day, and year. Movement from field to field is accomplished with the "ENTER" key. Values are changed using the "+/-" keys.

Legacy Diskette A: This option allows for setting the type of the first floppy drive attached. If no drive is attached, "disabled" should be selected. The option list is shown here:

- Disabled
- 360KB 5 ¼"
- 1.2MB 5 ¼"
- 720KB 3 ½"
- 1.44/1.25MB 3 ½"
- 2.88MB 3 ½"

Legacy Diskette B: This option allows for setting the type of the second floppy drive attached. If no drive is attached, "disabled" should be selected. The option list is shown here:

- Disabled
- 360KB 5 ¼"
- 1.2MB 5 ¼"
- 720KB 3 ½"
- 1.44/1.25MB 3 ½"
- 2.88MB 3 ½"

Primary Master: This option sets the drive type for the first fixed disk. Unlike older systems with fixed drive type numbers, the Phoenix BIOS relies primarily on the self-identification feature of modern IDE drives. This allows the BIOS to auto-detect the drive type and parameters. Support is also provided for user defined drive parameter definitions as well as support for Bootable CD-ROMs and removable ATAPI drives. The selection choices for this menu option are:

- Auto
- None
- CD-ROM
- ATAPI Removable
- User

When no fixed disk is to be attached, select "None" to minimize startup time. The "Auto" mode is the most versatile and works with nearly all modern hard disks, CD-ROMs and ATAPI-Removable drives.

Primary Slave: This option sets the drive type for the second fixed disk. Unlike older systems with fixed drive type numbers, the Phoenix BIOS relies primarily on the self-identification feature of modern IDE drives. This allows the BIOS to auto-detect the drive type and parameters. Support is also provided for user defined drive parameter definitions as well as supported for Bootable CD-ROMs and removable ATAPI drives. The selection choices for this menu option are:

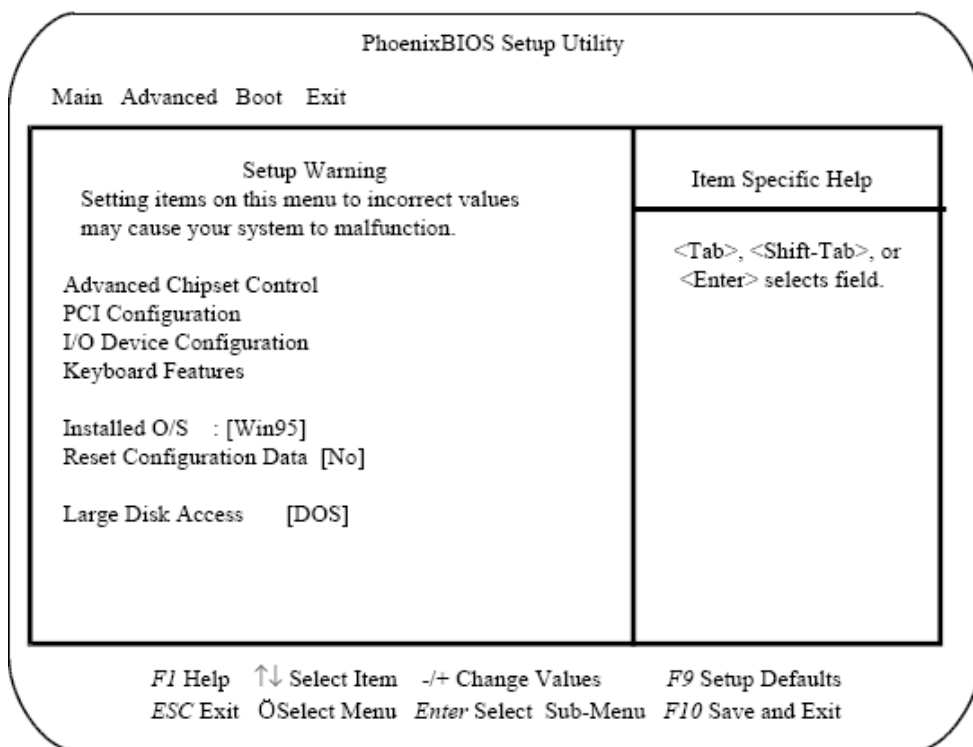
- Auto
- None
- CD-ROM
- ATAPI Removable
- User

When no fixed disk is to be attached, select "None" to minimize startup time. The "Auto" mode is the most versatile and works with nearly all modern hard disks, CD-ROMs and ATAPI-Removable drives.

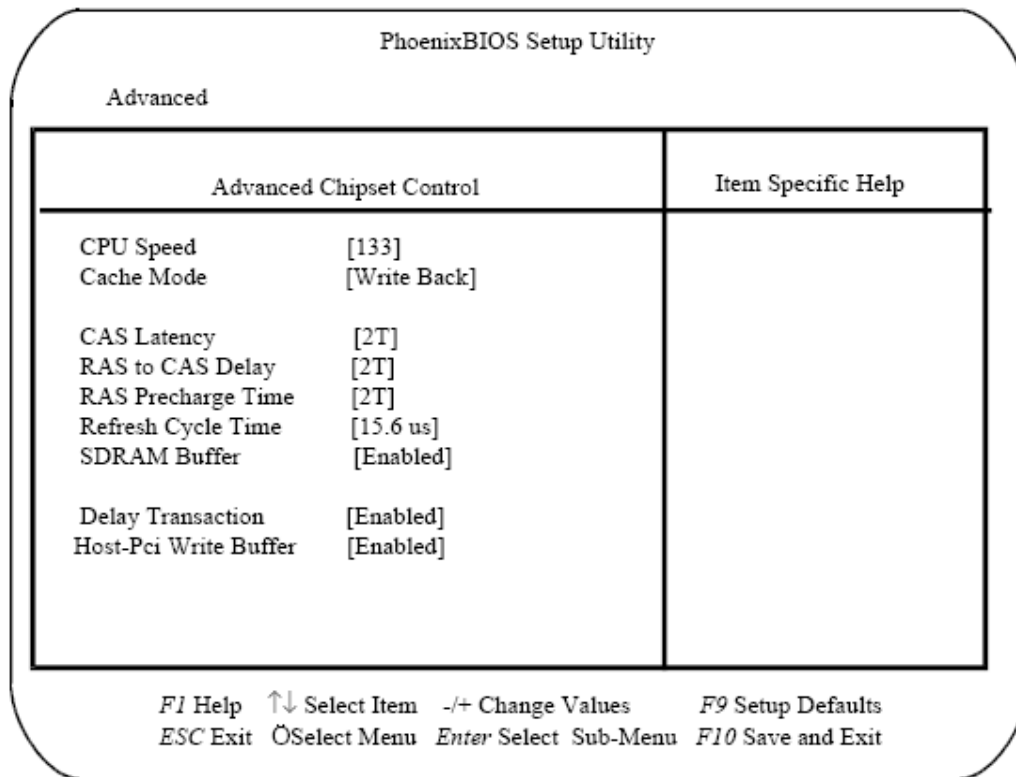
System Memory: This field is displayed by the BIOS and cannot be changed. It shows the amount of memory below 1MB that the system found.

Extended Memory: This is also a display only field. It represents the amount of extended memory above 1MB that was found in the system.

Advanced CMOS Setup – The advanced CMOS setup allows for the configuration of all of the non-disk related Setup items. There are several sub-menus that allow control of a number of systems and chipset features. Each of the setup options will be discussed in the sections that follow.



Advanced Chipset Control Menu - This submenu allows configuration of the chipset portion of the AMD SC520 processor/chipset. Each of the selections will be discussed in the following sections.



CPU Speed: This options allows for setting the CPU operating speed. In all cases the frequency is 33MHz and it is the internal CPU divisor that is changed by this option. The choices are:

- 133 MHz
- 100 MHz

Cache Mode: The SC520 has an on chip 16KB cache. The cache mode may be configured using this setup menu option. The options are:

- Write Back
- Write Through

CAS Latency: This selection allows the cache latency time to be varied by a number of (T) clock cycles. The available choices are:

- 3T
- 2T

RAS to CAS Delay: This selection allows for control of the RAS to CAS timing delay. It too is expressed in clock (T) cycles. The choices are:

2T
3T
4T

RAS Precharge Time: This selection controls the precharge time for DRAM cycles. The selections are expressed in clock (T) cycles. The available selections are:

2T
3T
4T
6T

Refresh Cycle Time: This selection allows control of the SDRAM refresh timing. This selection must match the requirements of the SDRAM actually installed. The available selections are:

7.8us
15.6us
31.2us
62.5us

SDRAM Buffer: This option allows for enabling or disabling the SDRAM buffer function. The available choices are:

Enabled
Disabled

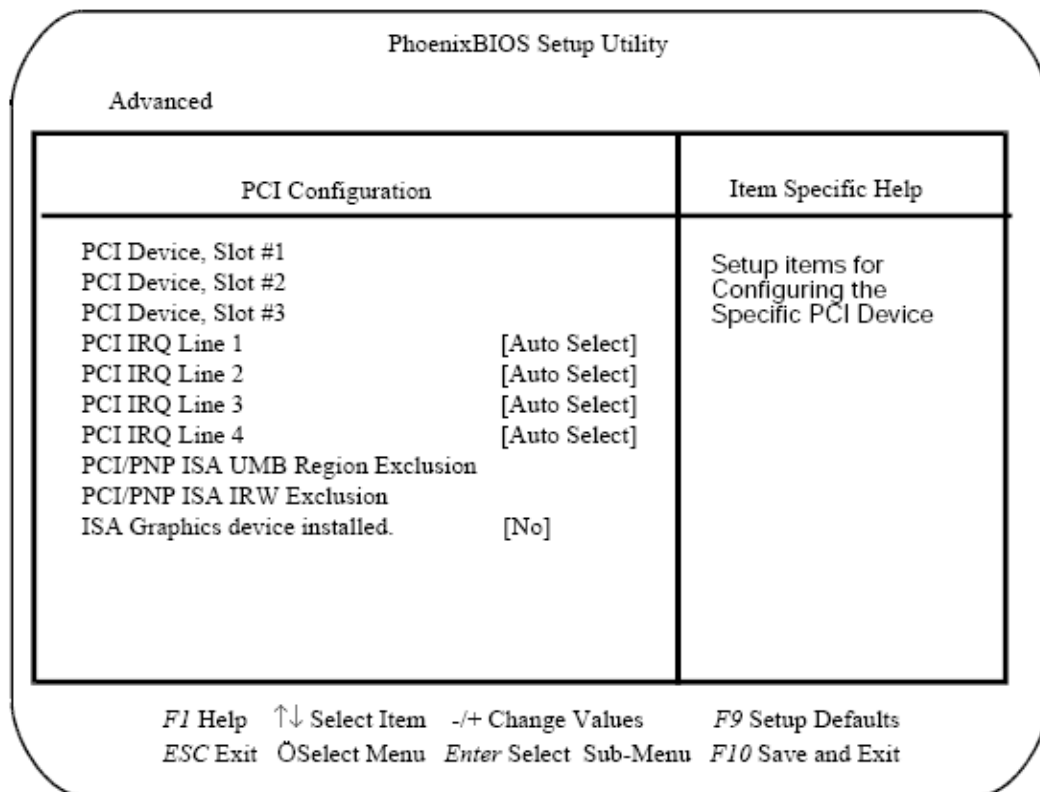
Delay Transaction: This selection allows for configuring the delayed transaction processing feature. The choices are:

Enabled
Disabled

Host-PCI Write Buffer: This selection allows for control of the Host-PCI write buffer. The selections are:

Enabled
Disabled

PCI Configuration – This menu allows setup configuration of the PCI bus resources. This menu should only be used by knowledgeable users. It is possible to configure the PCI resources so as not to allow the onboard peripherals to function due to lack of resources. The sections that follow describe each of the menu items and selections.



PCI Device, Slot #1: This submenu allows control of several parameters relating to modules attached as the PCI Slot 1 device. These include:

Option ROM Scan: If the PCI device contains a BIOS extension, its scan can be controlled using this option.

Enable Master: This options allows the device to serve as a PCI bus master if enabled.

Latency Timer: This selection controls the latency timer value. The choices are:

Default	0080H
0020H	00A0H
0040H	00C0H
0060H	00E0H

PCI Device, Slot #2: This submenu allows control of several parameters relating to modules attached as the PCI Slot 2 device. These include:

Option ROM Scan: If the PCI device contains a BIOS extension, its scan can be controlled using this option.

Enable Master: This options allows the device to serve as a PCI bus master if enabled.

Latency Timer: This selection controls the latency timer value. The choices are:

Default	0080H
0020H	00A0H
0040H	00C0H
0060H	00E0H

PCI Device, Slot #3: This submenu allows control of several parameters relating to modules attached as the PCI Slot 3 device. These include:

Option ROM Scan: If the PCI device contains a BIOS extension, its scan can be controlled using this option.

Enable Master: This options allows the device to serve as a PCI bus master if enabled.

Latency Timer: This selection controls the latency timer value. The choices are:

Default	0080H
0020H	00A0H
0040H	00C0H
0060H	00E0H

PCI IRQ Line 1: This option selects the IRQ to be routed to IRQ Line 1(A). The choices are:

Disabled	9
Auto Select	10
3	11
4	12
5	14
7	15

PCI IRQ Line 2 This option selects the IRQ to be routed to IRQ Line 2(B). The choices are:

Disabled	9
Auto Select	10
3	11
4	12
5	14
7	15

PCI IRQ Line 3: This option selects the IRQ to be routed to IRQ Line 3(C). The choices are:

Disabled	9
Auto Select	10
3	11
4	12
5	14
7	15

PCI IRQ Line 4: This option selects the IRQ to be routed to IRQ Line 4(D). The choices are:

Disabled	9
Auto Select	10
3	11
4	12
5	14
7	15

PCI/PnP ISA UMB Region Exclusion: This menu options allows specific upper memory blocks to be reserved so that they will not be used by PCI or ISA PnP devices. There are 6 address blocks that may be individually selected as either 'Available' or 'Reserved'. These blocks are:

C800 – CBFF	D400 – D7FF
CC00 – CFFF	D800 – DBFF
D000 – D3FF	DC00 – DFFF

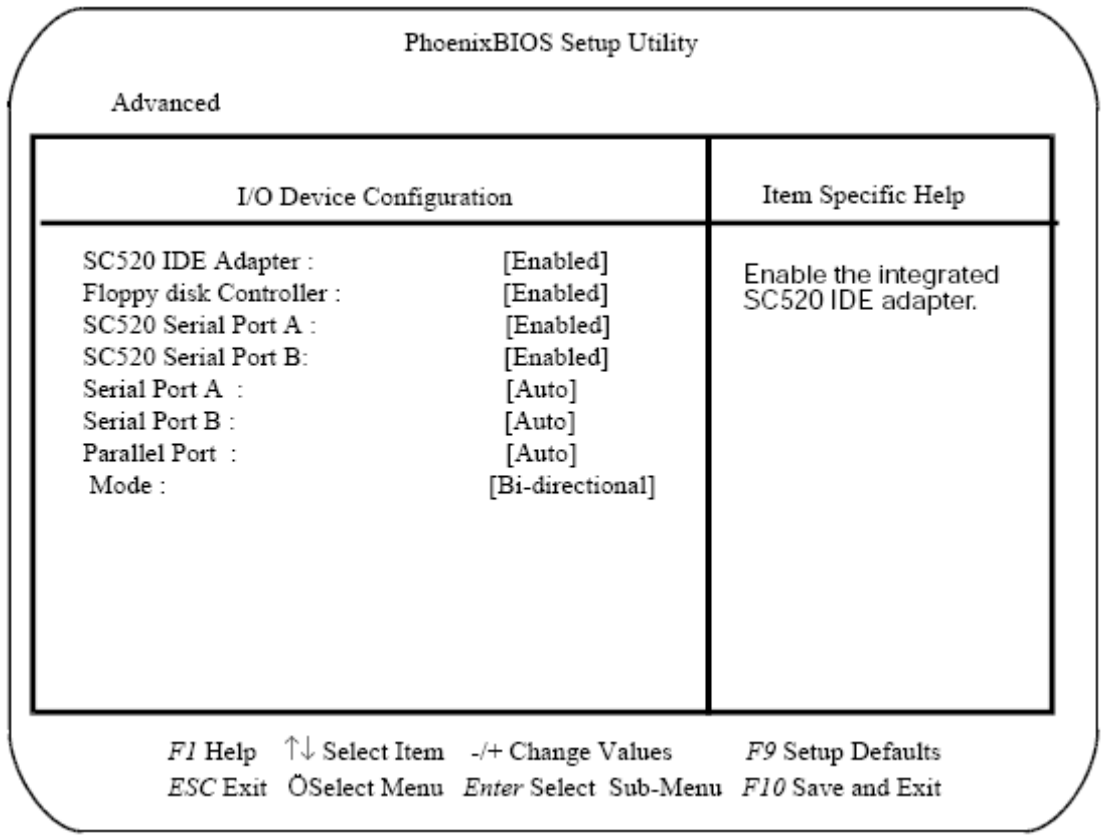
PCI/PnP ISA IRQ Resource Exclusion: This option, like the previous one, allows a resources (IRQ) to be reserved so that it will not be assigned to a PCI or ISA PnP device. Each of the listed IRQs may either be selected as 'Available' or 'Reserved'. The selectable IRQ resources are:

IRQ3	IRQ9
IRQ4	IRQ10
IRQ5	IRQ11
IRQ7	IRQ15

ISA Graphics Device Installed: This options when selected 'YES' allows a ISA (non-VGA) graphics device to access palette data in the PCI VGA device. The options are:

YES
NO

I/O Device Configuration – This menu allows configuration of a number of peripheral devices. Each of the menu options will be discussed in the sections that follow.



SC520 IDE Adapter: This configuration option controls the internal IDE interface. The options are:

- Enabled
- Disabled

When no IDE devices are connected, turning this option to 'Disabled' will result in a significant reduction in the time to boot.

Floppy Disk Controller: This option controls the floppy disk controller. The options are:

- Enabled
- Disabled

SC520 Serial Port A: This options configures the first serial port (COM1). The selection options for this menu item are:

- Enabled
- Disabled

SC520 Serial Port B: This options configures the second serial port (COM2). The selection options for this menu item are:

- Enabled
- Disabled

Serial Port A: This option controls the first serial port in the SMSC 37C727 super I/O chip (COM3). The available selections are:

- Disabled
- Enabled
- Auto
- OS Controlled

When the port is selected as 'Enabled", two submenu choices become visible.

Base I/O Address – This selection configures the base I/O address. The choices are:

- 3E8H
- 2E8H
- 3A8H
- 2A8H

Interrupt - This selects the desired interrupt for this port. The selections are:

- IRQ9
- IRQ11

Serial Port B: This option controls the first serial port in the SMSC 37C727 super I/O chip (COM3). The available selections are:

- Disabled
- Enabled
- Auto
- OS Controlled

When the port is selected as 'Enabled", two submenu choices become visible.

Base I/O Address – This selection configures the base I/O address. The choices are:

- 3E8H
- 2E8H
- 3A8H
- 2A8H

Interrupt - This selects the desired interrupt for this port. The selections are:

IRQ9
IRQ11

Parallel Port: This option controls the configuration of the onboard printer port. The available selections are:

Disabled
Enabled
Auto
OS Controller

Mode – This submenu allows selection of the parallel port operating mode. The selections are:

Output only
Bi-directional
EPP
ECP

When the port is selected as 'Enabled', two submenu choices become visible.

Base I/O Address – This selection configures the base I/O address. The choices are:

378
278
3BC

Interrupt - This selects the desired interrupt for this port. The selections are:

IRQ5
IRQ7

Keyboard Features: This menu enables configuration of the keyboard operating parameters. There are four items on this menu. Each of the selections will be discussed in the section that follows.

Numlock: This option determines the status of the Numlock LED. The available options are:

Auto
On
Off

Key Click: This selection enables or disables the sound produced when a key is pressed. The options are:

Disabled
Enable

Keyboard Auto Repeat Rate: This option controls the repeat rate (typematic) when a key is held down. The options are:

30/sec	13.3/sec
26.7/sec	10/sec
21.8/sec	6/sec
18.5/sec	2/sec

Keyboard Auto Repeat Delay: This options controls the time that a key must be held down before it begins to repeat. The selections are:

¼ sec	¾ sec
½ sec	1 sec

Miscellaneous Functions: The following items are also present on the Advanced Setup Menu.

Installed OS: This feature allows for the selection of O/S type. The selections are:

Win95
Other

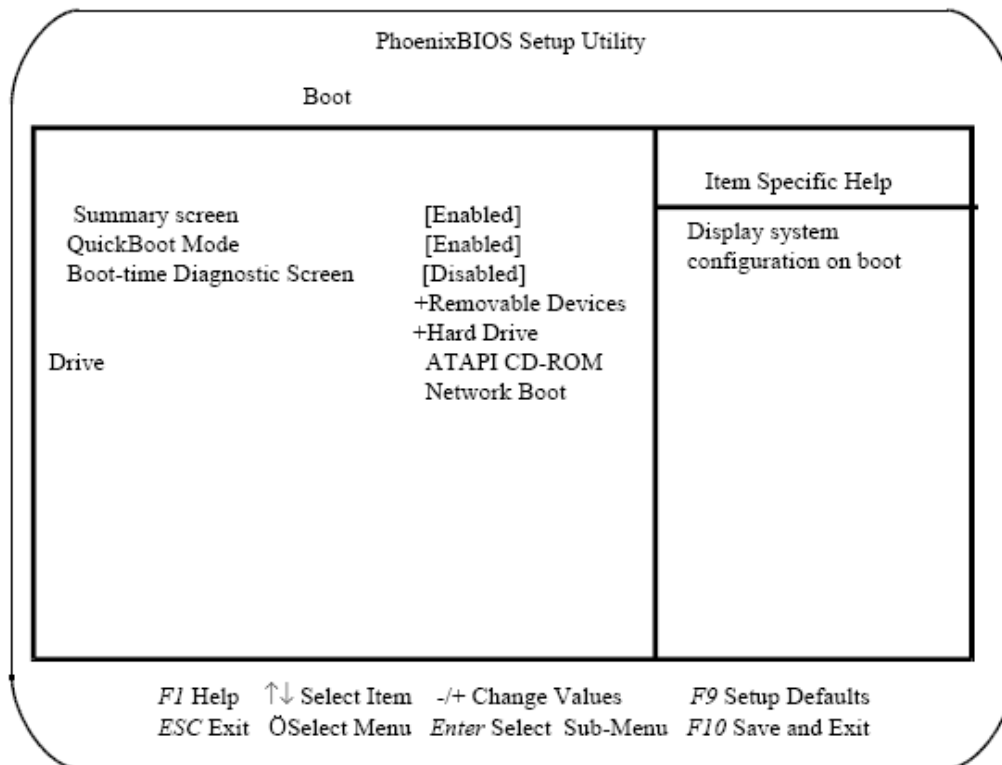
Reset Configuration Data: This option when enabled, resets the PnP and other configuration data which may be programmed by the BIOS into its flash memory. This will cause all devices and settings to be fully enumerated at the next boot. The available options are:

Yes
No

Large Disk Access: This options sets the large disk (greater than 529MB) access mode. The available selections are:

Other
DOS

Boot Setup – This menu allows selection of a number of Boot Options. Each of the menu items will be described in the following sections.



Summary Screen: This option allows for control of the system summary screen. When enabled, a configuration box will be displayed for three seconds prior to boot. The selection options are:

- Enabled
- Disabled

QuickBoot Mode: This option allows for a shortened POST process. When this option is 'Enabled' the memory test is shortened significantly, reducing the time to boot. The choices are:

- Disabled
- Enabled

Boot-time Diagnostic Screen: This option allows control of the Splash screen and the BIOS post and sign-on messages. When 'Enabled', the splash screen is off, and the BIOS messages will be displayed. Refer to the section on the Logo utility for information on creating custom BIOS splash screens. The choices are:

- Disabled
- Enabled

Boot Order: This options allows the available boot devices to be ordered according to the desired boot priority. Removable devices (floppy), hard disks, CD-ROM drives, and network boot items may be moved up or down the priority list using the keys as shown on the boot menu screen.

Exit Setup – This menu screen is used for exiting the setup menu and for saving or discarding any changes made.

Exit Saving Changes: This option when selected saves all of the changes made to the CMOS RAM and exits the Setup utility. A warm start reboot is attempted. In some cases depending upon systems conditions and changes made, the restart will not be successful and either a power-down or a manual reset may be required.

Exit Discarding Changes: This options exits the Setup utility and restarts the system. Any changes made (other than Date/Time) will not be saved.

Load Setup Defaults: This options when selected loads the CMOS RAM with all factory defaults.

Discard Changes: This option removes any changes made but does not exit the setup utility.

Save Changes: This option saves all changes made to CMOS RAM but does not exit the Setup utility.

Phlash Utility – The Phoenix BIOS onboard the SAT-520Plus is stored in Flash memory. BIOS updates may be programmed onboard using the Phoenix Phlash utility. *Phlash.exe* is a DOS executable program that may be run from the command prompt such as: *Phlash bios.rom*

This will executes the *Phlash.exe* program and start reprogramming of the BIOS with the specified file, *BIOS.ROM*. The Phlash utility also requires the presence of the file *PLATFORM.BIN*. The utility can be run from floppy, hard disk, of DiskOnChip. In may also be run “in the blind” without keyboard or video present by adding its invocation into the *AUTOEXEC.BAT* file on the boot media.

Logo Utility – The *LOGO.EXE* utility combined with the *BMP2PGX.EXE* program and MS-Windows *PAINT.EXE* allows for the creation of a custom splash screen that will be displayed during the BIOS post process. The steps for creating a custom splash screen are:

1. In Windows Paint or another graphic utility capable of generating Windows .BMP files, create your desired screen with a resolution of 640 X 480 pixels in 16 colors. This resolution and color count must be adhered to if the graphic is to be displayed properly. Save the file in a .BMP format.
2. Run the *BMP2GPX.EXE* utility to convert the .BMP file to a .PGX file which is a compressed graphic format used by the Phoenix BIOS display manager. The invocation line is like this: **bmp2gpx.logo.bmp**

This will create the .PGX file required for the next step. The name will be the same as the .BMP file with a .PGX extension.

3. Run the *LOGO.EXE* utility to place the .PGX file into the BIOS image file. If the BIOS image file is named BIOS.ROM and the logo file is called *LOGO.PGX*, then the command: **logo bios.rom logo.pgx** will load the new logo file into the BIOS.ROM file at the proper position.
4. Use the *Phlash.exe* utility described in the previous section to program the new BIOS image.
5. Using the BIOS Setup, on the Boot Menu, disable the Boot-Time Diagnostic Screen.

During the POST routines, your screen will be displayed. You can still press <ESCAPE> to return the diagnostic screen of <F2> to enter setup.

I/O Port Map

The following is a list of PC I/O ports. Addresses marked with a '-' are not used on the SAT-502Plus but their use should be carefully evaluated so as not to conflict with other I/O boards. I/O addresses marked with a '+' are used on the SAT-520Plus and are unique to the WinSystems design. I/O addresses marked with '**' are generally unused and should be the basis for the first choices in I/O address selection for external I/O boards.

NOTE: The SAT-520Plus uses a PnP BIOS for both the PC/104Plus and the PC/104 bus I/O resource allocations. Care must be taken to avoid contention with resources allocated by the BIOS.

<u>HEX Range</u>	<u>Usage</u>	<u>HEX Range</u>	<u>Usage</u>
000-00F	8327 DMA Controller #1	**300-32F	Free
**010-01F	Free	370-377	Floppy Disk Controller #2
020-021	8259 PIC #1	378-37F	Parallel Printer
**022-03F	Free	**380-3A7	Free
040-043	8254 PIT	3A8-3AF	Serial Port
**044-05F	Free	3B0-3BB	MDA
060-06F	8042 Keybrd/Mouse Control	3BC-3BF	Parallel Port
070-07F	CMOS RAM, Clock/Calendar	3C0-3CF	EGA/VGA
080-09F	DMA Page Registers	3D0-3DF	CGA
0A0-0BF	8259 PIC #2	**3E0-3E7	Free
0C0-0DF	8237 DMA Controller #2	3E8-3EF	Serial Port
**0E0-0EF	Free	3F0-3F7	Floppy Disk Controller #1
0F0-0F1	Math Coprocessor Control	3F8-3FF	Serial Port
**0F2-0F7	Free		
085-0FF	Math Coprocessor		
100-102	VGA Control Register		
**103-16F	Free		
170-177	IDE Controller #2		
**178-1EC	Free		
+1ED-1EF	Watchdog/LED Control		
1F0-1FF	IDE Controller #1		
200-207	Game Port		
**208-237	Free		
238-23B	Bus Mouse		
23C-23F	Alt. Bus Mouse		
**240-277	Free		
278-27F	Parallel Port		
**280-2a7	Free		
2A8-2AF	Serial Port		
2B0-2BF	EGA		
2C0-2CF	EGA		
2D0-2DF	EGA		
2E0-2E7	GPIB Interface		
2E8-2EF	Serial Port		
**2F0-2F7	Free		
2F8-2FF	Serial Port		

Interrupt Map

<u>No.</u>	<u>Address</u>	<u>Type</u>	<u>Description</u>
0	0	CPU	Divide by Zero
1	4	CPU	Single Step
		386+	Debug Exception
2	8	CPU	NMI
3	0C	CPU	Breakpoint
4	10	CPU	Overflow
5	14	BIOS	Print Screen
		186+	Bounds Exception
6	18	186+	Invalid Opcode
7	1C	186+	Coprocessor unavailable
8	20	HARDWARE	IRQ 0 - 18.2Hz heartbeat
		286+	LIDT - Double fault exception
9	24	HARDWARE	IRQ 1 - Keyboard
		286+	Coprocessor segment
A	28	HARDWARE	IRQ 2 - Chained to slave
		286+	Invalid TSS exception
B	2C	HARDWARE	IRQ 3 - COM2
		286+	Segment not present
C	30	HARDWARE	IRQ 4 - COM1
		286+	Stack fault exception
D	34	HARDWARE	IRQ 5
		286+	Protection Fault
E	38	HARDWARE	IRQ 6 - Floppy Disk
		286+	Page fault
F	3C	HARDWARE	IRQ 7 - LPT 1
10	40	BIOS	Video BIOS functions
		286+	Coprocessor exception
11	44	BIOS	BIOS equipment check
		486+	Alignment check exception
12	48	BIOS	BIOS memory size
		P5+	Machine check
13	4C	BIOS	BIOS disk function
14	50	BIOS	BIOS serial functions
15	54	BIOS	BIOS cassette/misc functions
16	58	BIOS	BIOS keyboard functions
17	5C	BIOS	BIOS printer functions
18	60	BIOS	SROM Basic Entry (IBM)
19	64	BIOS	BIOS Boot function
1A	68	BIOS	BIOS time of day functions
1B	6C	BIOS	BIOS keyboard break
1C	70	BIOS	BIOS chained timer tick
1D	74	BIOS	BIOS video initialization
			BIOS diskette parameter table
1E	78	BIOS	
1F	7C	BIOS	BIOS CGA graphics fone
20	80	MS-DOS	Program Terminate
21	84	MS-DOS	DOS function calls
22	88	MS-DOS	Terminate address
23	8C	MS-DOS	Ctrl-Break address
24	90	MS-DOS	Fatal Error vector
25	94	MS-DOS	Absolute disk read
26	98	MS-DOS	Absolute disk write
27	9C	MS-DOS	Terminate address

<u>No.</u>	<u>Address</u>	<u>Type</u>	<u>Description</u>
28	A0	MS-DOS	Idle signal
29	A4	MS-DOS	TTY output
2A	A8	MS-DOS	MS-Net services
2F	BC	MS-DOS	Print Spool
30	C0	MS-DOS	Long jump interface
33	CC	MS-DOS	Mouse functions
3F	FC	MS-DOS	Overlay interrupt
40	100	BIOS	BIOS floppy redirect
41	104	BIOS	BIOS Fixed disk 1 table
42	108	BIOS	EGA Chain
43	10C	BIOS	EGA Parameter table pointer
44	110	BIOS	EGA graphics font
46	118	BIOS	BIOS Fixed disk 2 table
4A	128	BIOS	AT Alarm exit address
50	140	BIOS	AT Alarm interrupt
51	144	BIOS	Mouse functions
5A	168	NET	NET functions
5B	16C	NET	boot chain
5C	170	NET	NET BIOS entry
67	19C	MS-DOS	EMS functions
6D	1B4	VGA	VGA service
70	1C0	HARDWARE	IRQ 8 - Real time clock
71	1C4	HARDWARE	IRQ 9 - Redirected IRQ 2
72	1C8	HARDWARE	IRQ 10 - unassigned
73	1CC	HARDWARE	IRQ 11 - unassigned
74	1D0	HARDWARE	IRQ 12 - Mouse
75	1D4	HARDWARE	IRQ 13 - Coprocessor
76	1D8	HARDWARE	IRQ 14 - IDE hard disk
77	1DC	HARDWARE	IRQ 15 - unassigned

Datasheet Reprint

Intel 82C55A	intel_82c55a.pdf
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Cables

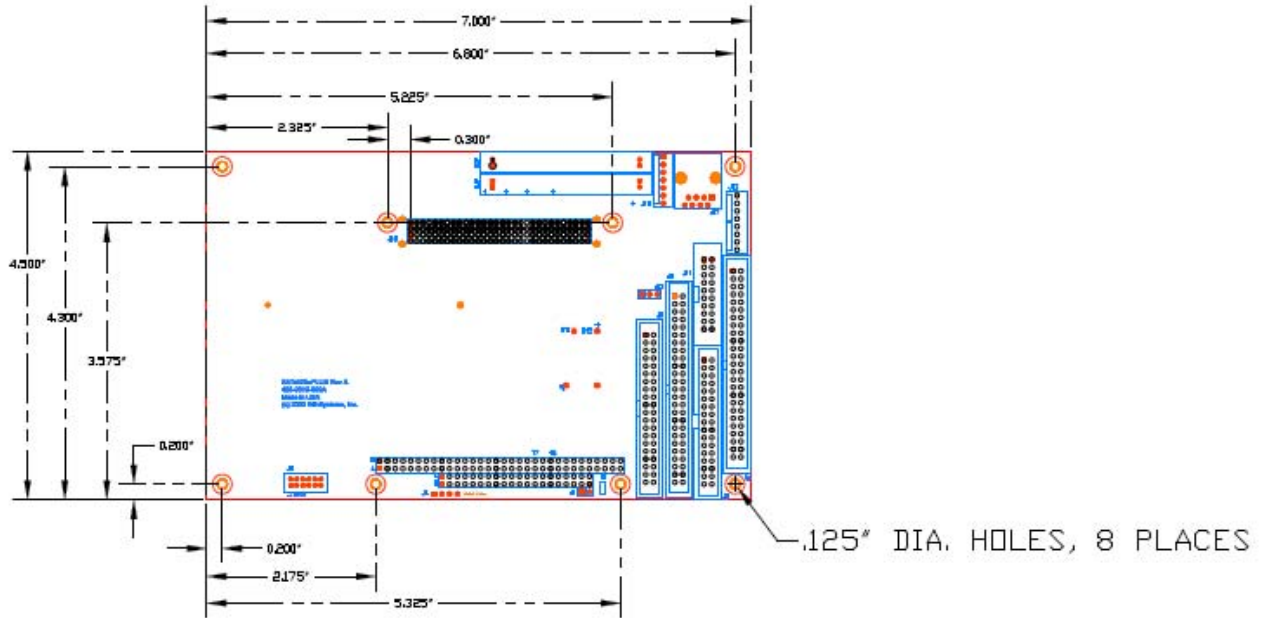
Part Number	Description
CBL-115-4	50-pin 4ft. Opto Rack interface cable
CBL-125-1	Floppy Disk Adapter Cable
CBL-173-1	20-pin ribbon to two DB-9 for serial channels 3&4
CBL-174-1	Power cable for sbc (unterminated)
CBL-225-1	PS/2 mouse adapter cable
CBL-234-1	CRT adapter cable - 14-pin ribbon to 15-pin D-sub
CBL-247-1	Multi-I/O adapter cable PS/2 keyboard, serial 1&2, and LPT

Software Drivers & Examples

Latest BIOS and Utilities	sat520_rel0920.zip
Drivers for Assilant (Chips & Technology) 69000 Video Controller	
Driver for Windows XP	wxpv251c.zip
Driver for Windows 2000	w2kv251c.zip
Driver for Windows NT 4.0	nt4v251c.zip
Driver for Windows 3.1	w31132.zip
Driver for Windows 95	w95500.zip
Driver for Windows 98	w98600.zip
Driver for OS/2 3.0 & 4.0	os2231.zip
Initialization routine for 82C55 (Assembly Language)	8255init.zip
Drivers for Intel 82551ER/82559ER 10/100 Ethernet Controller	
Linux Kernels - 2.4.x & 2.6.x kernels	e100-3.5.14.tar.gz
Latest known to compile for 2.2.x kernels	e100-2.1.15.tar.gz
NDIS4 (Windows 98)	82559erWin98.zip
NDIS4 (Windows NT 4 & 2000)	e100ndis4.zip
Windows NT Embedded 4.0	e100ent.zip
Windows XP/2000	e100exp.zip
Windows CE 3.0	e100ce3.zip
Linux Drivers	
Kernel 2.2, 2.4	linux_uio48_96.zip
Kernel 2.6	uio48io_kernel_2.6.zip
Windows XP Driver	wsuio48_96xp.zip
Example of reprogramming DOS tick for high resolution timing	tickdemo.zip
Serial Console Utilities:	
Generic 38400baud Serial console redirect for COM1	scon1.zip

Generic 38400baud Serial console redirect for COM2	scon2.zip
Generic 9600baud Serial console redirect for COM1	sc19600.zip
Generic 9600baud Serial console redirect for COM2	sc29600.zip

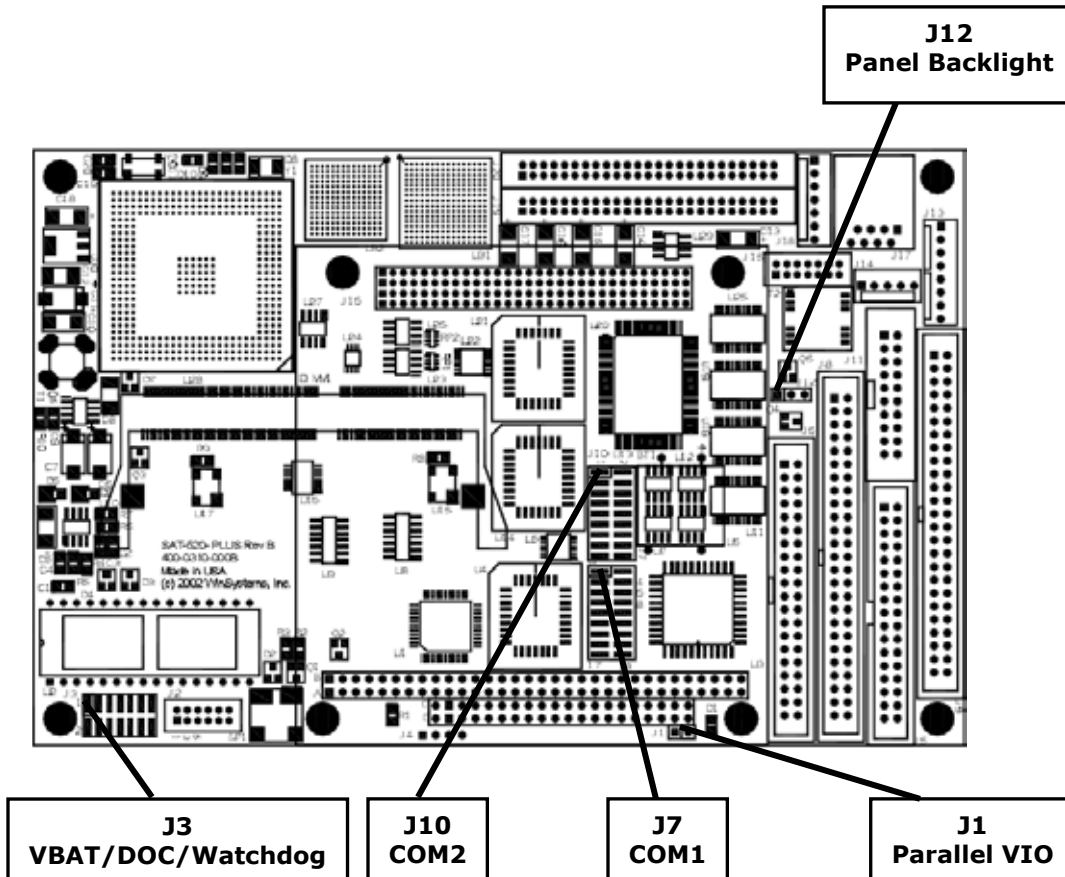
Mechanical Drawing



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE FRACTIONS ANGLES 4/± 1/2" DECIMALS .001 ± .005 .002 ± .003	CUSTOMER APPROVAL	DATE	WinSystems, Inc. "THE STD BUS AUTHORITY" SAT-520PLUS MOUNTING DIMENSIONS	
	APPROVAL	DATE		
MACHINE FINISH ✓	CHECKER	DATE	SIZE	WGE CODE
	DRAFT/DESIGN M.BROWNING	DATE 11/19/02	C	1A007
			DWG NO.	REV
			SAT520PLUS.DWG	A
			SCALE	CAD OR SAT520PLUS.DWG SHEET 1 OF 1

Jumper Reference

Drawings ONLY - for more detailed information on these parts, refer to the descriptions shown previously in this manual.



J3

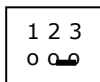
1	3	5	7	9	11	13
0	0	0	0	0	0	0
0	0	0	0	0	0	0
2	4	6	8	10	12	14

- 3-5 watchdog enabled in software
- 5 6 watchdog enabled (NOT compatible with Phoenix BIOS or with MS-DOS)
- 5-6 watchdog disabled
- 7-8 DOC enabled
- 7 8 DOC disabled
- 13-14 DIO enabled
- 13 14 DIO disabled

COM1/COM2 (J7 and J10)

Mode #	Description	Jumpers	Termination		
			TX (100)	RX (100)	TX/RX (300)
1	RS-232	1-2	N/A	N/A	N/A
2	RS-422 RTS Enable	3-4, 9-10	11-12	17-18	11-12 13-14 15-16
3	RS-422 Auto Enable	3-5, 9-10 (One node must use TX/RX 300 Termination)	N/A	17-18	11-12 13-14 15-16
4	RS-485 RTS Enable	3-4, 7-8	11-12	N/A	11-12 13-14 15-16
5	RS-485 RTS Enable with Echo-Back	3-4, 8-6	11-12	N/A	11-12 13-14 15-16
6	RS-485 Auto Enable	3-5, 7-8 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16
7	RS-485 Auto Enable with Echo-Back	3-5, 8-6 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16

J12



panel backlight enabled

J1



+5V supplied to J8, pin 49 (Parallel I/O)

Specifications

Electrical

Bus Interface	: PC/104 8-bit or 16-bit expansion bus PC/104-Plus 32-bit expansion bus
System Clock	: 33MHz
PCI Clock	: 33 MHz
VCC	: +5V \pm 5% at 1200mA typical with 256Mbytes SDRAM installed
VCC1	: +12V \pm 5% (not required. PC/104 Expansion Only)
VCC2	: -12V \pm 5% (not required. PC/104 Expansion Only)

Memory

Addressing	: 256MByte Addressing
BIOS	: 512KByte Flash
SDRAM	: 32 to 256 MByte SDRAM SODIMM with gold fingers (PC100 to PC133)
SSD	: M-Systems 32-pin DiskOnChip (8Mb to 288Mb)

Mechanical

Dimensions	: 4.5" x 7.1" x .60" (without expansion modules or cables)
PC-Board	: FR-4 Epoxy Glass with 6 signal layers and 2 power planes with screened component legend, and plated through holes
Jumpers	: AMDebug: 0.025" square posts on 0.10" centers Others: 0.5mm square posts on 2 mm centers
Connectors	: Multi-I/O: 50-pin RN type IDH-50-LP COM3/COM4: 20-pin RN type IDH-50-LP Floppy Disk: 34-pin RN type IDH-50-LP IDE Disk: 40-pin RN type IDH-50-LP CRT: 144-pin 2mm Molex type 87331-1420 Flat Panel: two, 50-pin 2mm Molex type 87331-5020 PC/104 Bus: 64-pin SAMTEC type ESQ-132-12-G-D 40-pin SAMTEC type ESQ-120-12-G-D PC/104-Plus Bus: SAMTEC type TS-30Q Power/Reset: 8-pin Molex type 22-11-2082 Parallel I/O: 50-6-pin RN type IDH-50-LP
Weight	:

Environmental

Operating Temperature	: -40°C to +85°C
Non-Condensing Relative Humidity	: 5 to 95%
MTBF	: 12.30 years

WARRANTY REPAIR INFORMATION

WARRANTY

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WARRANTY SERVICE

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.
2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.

