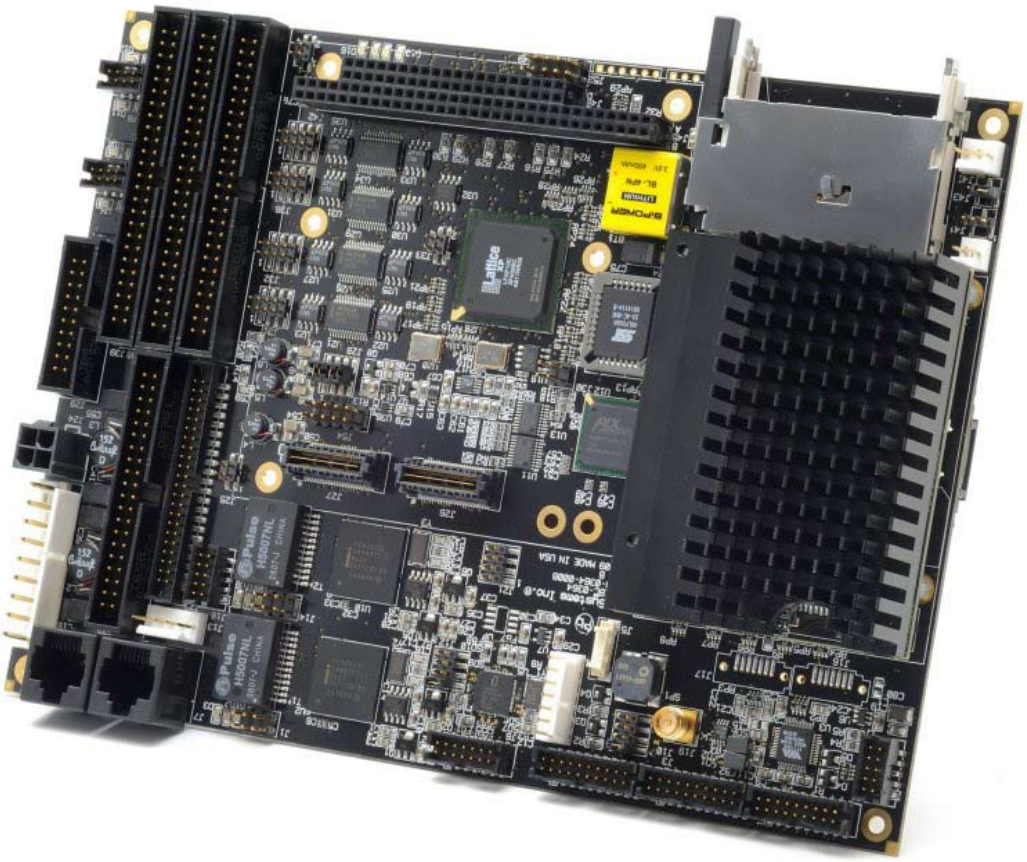
EBC-Z5xx

Intel® ATOM™ Single Board Computer

PRODUCT MANUAL



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MANUAL REVISION HISTORY

P/N 400-0364-000

Revision Date Code	ECO Number
101001	Initial Release
101213	10-75
110113	

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BEFORE YOU BEGIN

WinSystems offers best practice recommendations for using and handling WinSystems embedded PCs. These methods include valuable advice to provide an optimal user experience and to prevent damage to yourself and/or the product.

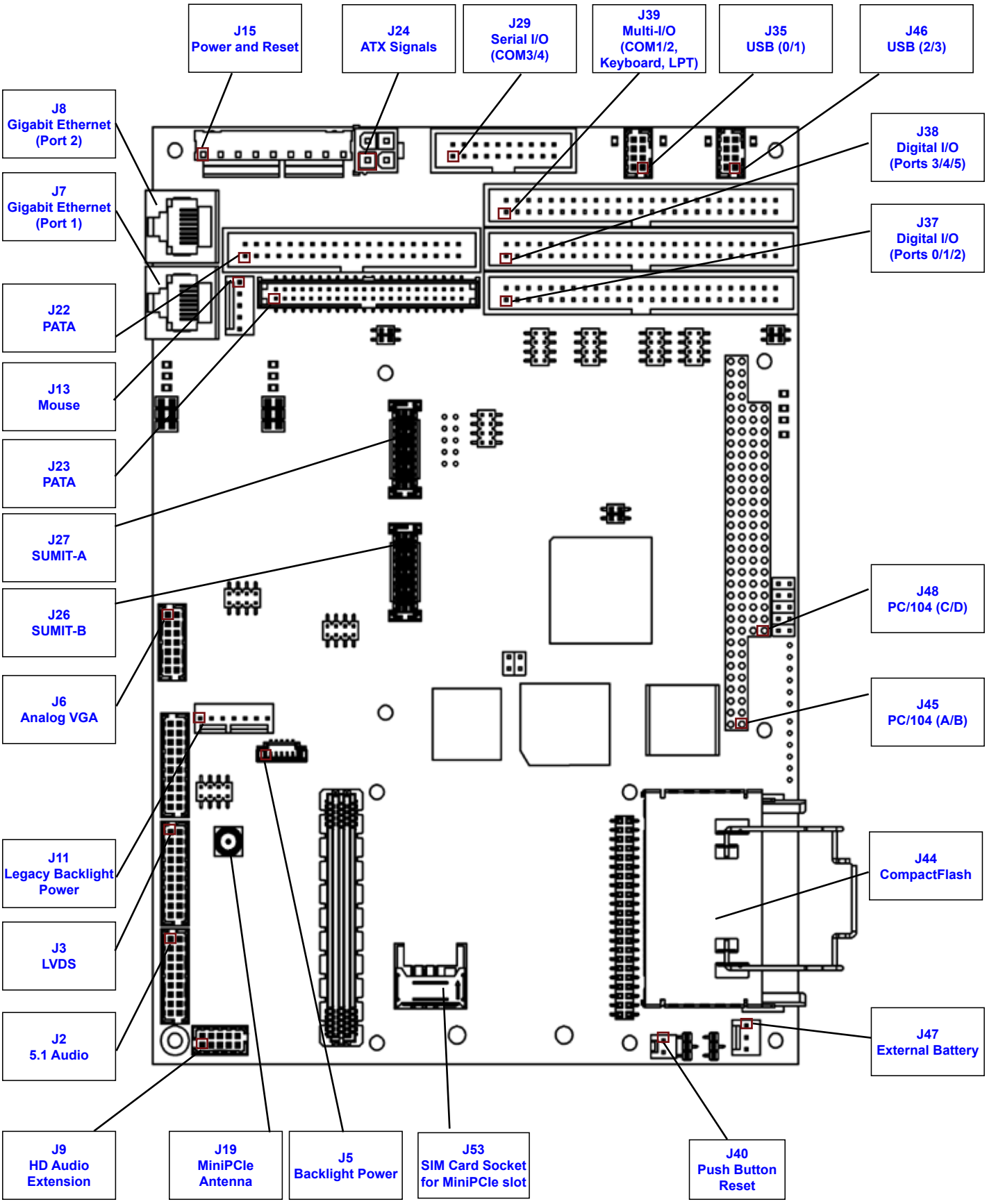
YOU MAY VOID YOUR WARRANTY AND/OR DAMAGE AN EMBEDDED PC BY FAILING TO COMPLY WITH THESE BEST PRACTICES.

Reference **Appendix - A** for **Best Practices**.

Please review these guidelines carefully and follow them to ensure you are successfully using your embedded PC.
This product ships with a heat sink. Product warranty is void if the heat sink is removed from the product.

For any questions you may have on WinSystems products, contact our Technical Support Group at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

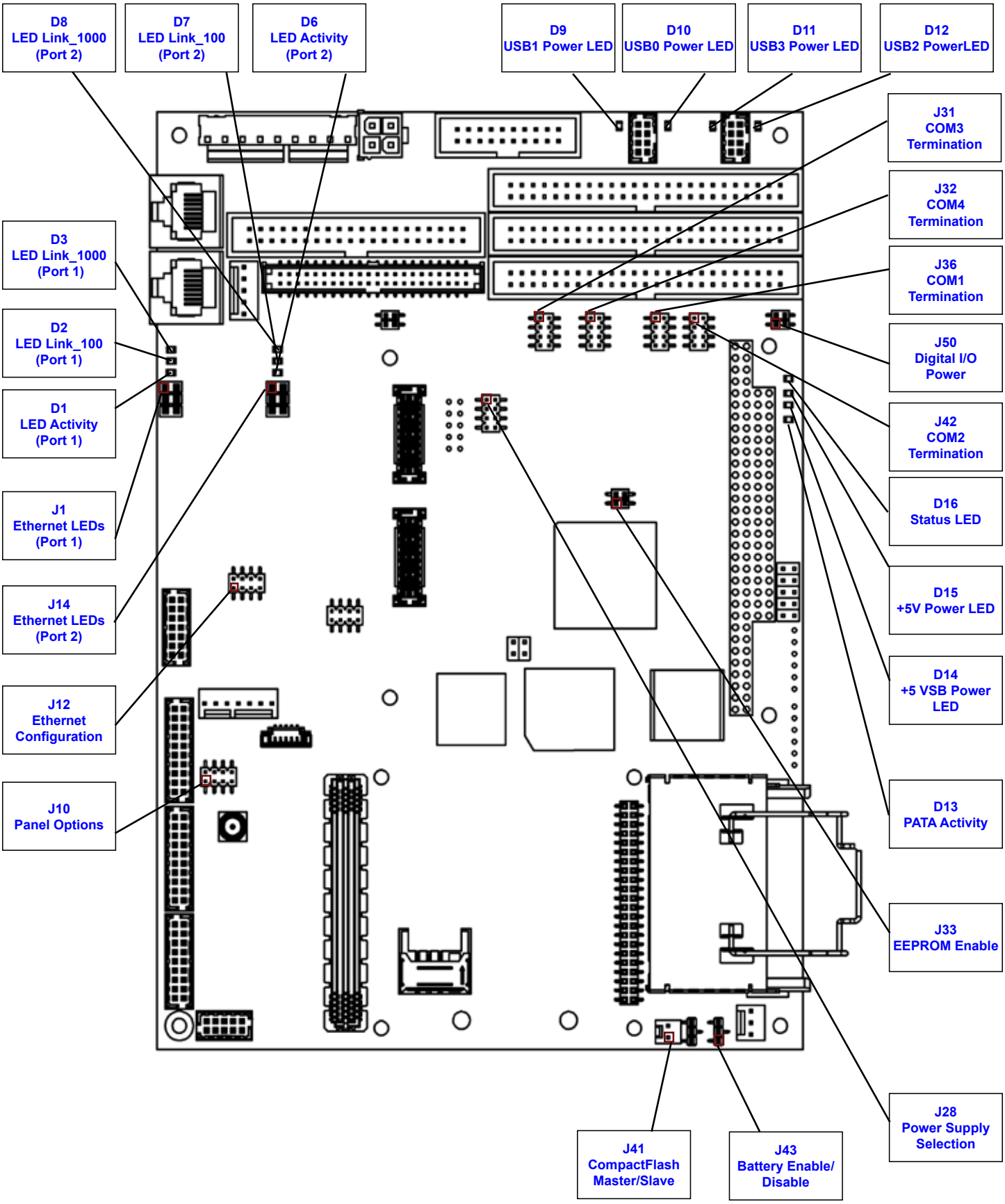
Visual Index - Top View (Connectors)



RESERVED - J4, J16, J17, J18, J20, J21, J24, J34, J44, J51, J52, J54, J103, D111, D112

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

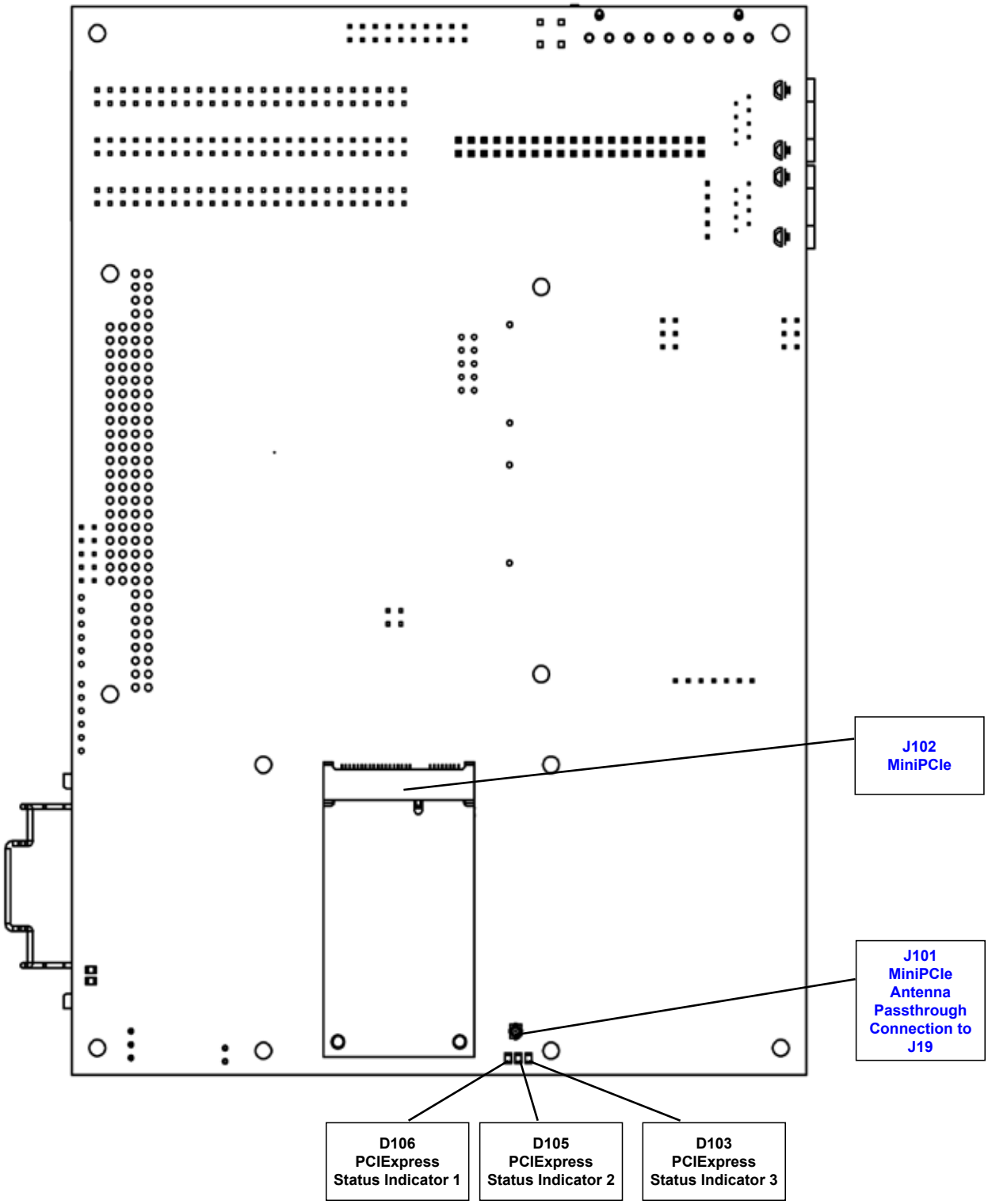
Visual Index - Top View (Jumpers & LEDs)



RESERVED - J4, J16, J17, J18, J20, J21, J24, J34, J44, J51, J52, J54, J103, D111, D112

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Visual Index - Bottom View (Connectors, Jumpers & LEDs)



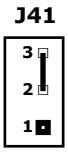
RESERVED - J4, J16, J17, J18, J20, J21, J24, J34, J44, J51, J52, J54, J103, D111, D112

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Jumper Reference

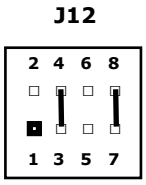
NOTE: Jumper Part# SAMTEC 2SN-BK-G is applicable to all jumpers. These are available in a ten piece kit from WinSystems (Part# KIT-JMP-G-200).

J41 - CompactFlash



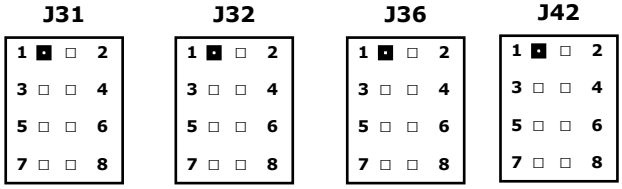
CompactFlash Master	1-2
CompactFlash Slave (default)	2-3

J12 - Ethernet Configuration



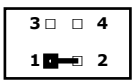
Ethernet Port 1	
Non-Volatile Memory Protection (Install Jumper to Disable Protection)	1-2
Auxiliary Power Present (Remove Jumper when powered in ATX Mode - Default Installed)	3-4
Ethernet Port 2	
Non-Volatile Memory Protection (Install Jumper to Disable Protection)	5-6
Ethernet Port 2 Present (If Ethernet Port 2 is not installed, remove jumper)	7-8

J31 - COM3, J32 - COM4, J36 - COM1, J42 - COM2



RS-422/RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		3-4
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	1-2
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	3-4
	Places a 100Ω Resistor from Ground to TX/RX-	5-6

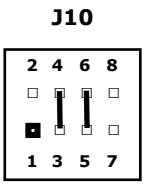
J33 - EEPROM



EEPROM Enable	
EEPROM Enabled (default)	1-2
EEPROM Disabled	3-4

Jumper Reference (cont'd)

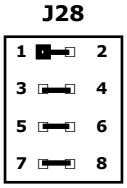
J10 - Panel Power



Avoid Simultaneous Jumpering of pins 1-2 and 3-4.
Misjumpering panel power causes damage to the board and/or the Flat Panel.

Panel Power	5V 3.3V (default)	1-2, 3 4 1 2, 3-4
Backlight Enable for J11	Active High Enable (default) Active Low Enable	5-6, 7 8 5 6, 7-8

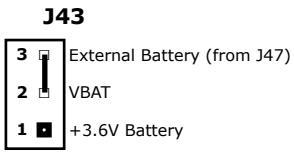
J28 - Power Supply Selection



AT Power	1-2, 3-4, 5-6, 7-8 (default)
ATX Power	1 2, 3 4, 5 6, 7 8

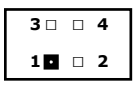
J43 - Battery (Enable/Disable)

Master Battery Enable



Enables On-board Battery	1-2
Enables External Battery (default)	2-3

J50 - Digital I/O VCC



Avoid Simultaneous Jumpering of pins 1-2 and 3-4.
Misjumpering causes damage to the board.

+3.3V is provided at pin 49 of **J37/J38**	3-4
+5V is provided at pin 49 of **J37/J38**	1-2
No Power at Pin 49 of **J37/J38** (default)	1 2, 3 4

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INTRODUCTION

This manual is intended to provide the necessary information regarding configuration and usage of the EBC-Z5xx single board computer. WinSystems maintains a Technical Support Group to help answer questions not adequately addressed in this manual. Contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

FEATURES

CPU
- Intel® ATOM™ Z510 (1.1 GHz) or Z530 (1.6 GHz)

Compatible Operating Systems
- Linux, Windows Embedded Standard, Windows XP, DOS, x86 RTOS

Memory
- 512 MB of DDR2 SDRAM (Soldered)

BIOS
- Phoenix

Video
- Analog VGA or Flat Panel operation (simultaneous operation)
- Analog VGA resolution up to 1920x1080
- Flat Panel resolution up to 1920x1080
- Up to 18-bits/pixel color panel
- LVDS

Ethernet
- 2 Intel® 10/100/1000 Mbps Gigabit controller (PC82573L)

Digital I/O
- 48 Bidirectional lines (WS16C48)

Serial I/O
- 4 serial ports (RS-232/422/485)

Line Printer Port
- SPP/EPP

USB
- 4 USB 2.0 ports

Watchdog Timer
- Up to 300 second reset

CompactFlash
- Types I & II

Audio
- HD Audio

Bus Expansion
- SUMIT
- PC/104
- MiniPCIe

Industrial Operating Temperature
- -40°C to 70°C (1.1 GHz)
- -40°C to 60°C (1.6 GHz)

Form Factor

- EBX-compliant
- 5.75” x 8.00” (147 mm x 203 mm)

Additional Features

- RoHS compliant
- Real-time clock/calendar
- Activity status LEDs on-board
- PS/2 Keyboard and Mouse

System

The EBC-Z5xx is an Intel® ATOM™ single board computer (SBC) which uses either an Intel 1.1 GHz (model EBC-Z510) or 1.6 GHz CPU (model EBC-Z530). This is an EBX-compatible unit and incorporates two Intel PC82573L Gigabit Ethernet controllers, supports the SUMIT interface, 48 lines of digital I/O, four serial RS-232/422/485 ports, watchdog timer, PS/2 keyboard and mouse controller, and LPT. The SBC also supports HD audio, USB ports, and is equipped with a CompactFlash socket and MiniPCIe card socket.

Memory

The EBC-Z5xx board is built with 512 MB of SDRAM soldered directly to the PCB.

FUNCTIONALITY

I/O Port Map

Following is a list of I/O ports used on the EBC-Z5xx. I/O addresses marked with a ** are generally unused and should be the first choice in I/O address selection for external I/O boards.

NOTE: The EBC-Z5xx uses a PnP BIOS resource allocation. Care must be taken to avoid contention with resources allocated by the BIOS.

HEX Range	Usage
020-03F	8259 Master
040-043	8254 PIT
04E-04F	Reserved for on-board configuration
050-053	8254
060-06F	Keyboard / Mouse Controller
070-07F	CMOS RAM, Clock / Calendar
084-08F	Internal / LPC
0A0-0BF	8259 Slave
0F0-0FF	Math Co-processor
**100-11F	Free
120-12F	Digital I/O
**130-14F	Free
150	Reserved for on-board configuration
**151-16F	Free
170-177	PATA
178-1CF	Free
1D0-1DF	Legacy Watchdog (1D0-Enabled; 1D8 - Pet)
1E8-1EB	Reserved for on-board configuration
1EC	Interrupt Status Register
1ED	Status LED
1EE-1EF	Watchdog Timer Control
1F0-1FF	PATA
**200-2AF	Free
2B0-2DF	Video Controllers
**2E0-2E7	Free
2E8-2EF	COM4 (Default)
**2F0-2F7	Free
2F8-2FF	COM2 (Default)
**300-375	Free
376-377	PATA
378-37B	LPT (Default)
**37C-3AF	Free
3B0-3BB	Video Controllers
**3BC-3BF	Free
3C0-3DF	Video Controllers
**3E0-3E7	Free
3E8-3EF	COM3 (Default)
**3F0-3F7	Free
3F6-3F7	PATA
3F8-3FF	COM1 (Default)
564-568	Advanced Watchdog
CF8-CFF	Internal Control Registers

Interrupt Map

Hardware Interrupts (IRQs) are supported for both PC/104 (ISA) and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS will use unreserved IRQs when allocating resources during the boot process. The table below lists IRQ resources as used by the EBC-Z5xx.

IRQ0	18.2 Hz heartbeat
IRQ1	Keyboard
IRQ2	Chained to Slave controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	COM3 *
IRQ6	COM4 *
IRQ7	LPT *
IRQ8	Real Time Clock
IRQ9	FREE **
IRQ10	Digital I/O
IRQ11	PCIe Interrupts
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	IDE
IRQ15	PCIe Interrupts

*	These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the Super I/O Control section under Intel.
**	IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.
***	IRQ15 is currently unavailable under the Windows operating systems.
Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.	

Interrupt Status Register - 1ECH

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	COM4	COM3	COM2	COM1

Note: A **1** will be read for the device(s) with an interrupt pending.

WinSystems does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts and examples are available. The user will need to implement the appropriate software to share interrupts for the other devices.

Watchdog Timer

The EBC-Z5xx features an advanced watchdog timer which can be used to guard against software lockups. Three interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other two interface options are provided for software compatibility with older WinSystems single board computers.

Advanced

The watchdog timer can be enabled in the BIOS Settings by entering a value for Watchdog Timeout on the Intel → Super I/O Control screen. Any non-zero value represents the number of minutes prior to reset during system boot. Once the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE: It is recommended that a long timeout be used if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. The watchdog is enabled by writing a timeout value other than zero to the I/O address 566h and disabled by writing **00h** to this I/O address. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value can be set from 1 second to 256 minutes. If port 565h bit 7 equals **0**, the timeout value written into I/O address 566h is in minutes. The timeout value written to address 566h is in seconds if port 565 bit 7 equals **1**.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565H	x	566H	00h	DISABLED
565H	1	566H	03h	3 SECONDS
565H	1	566H	1Eh	30 SECONDS
565H	0	566H	04h	4 MINUTES
565H	0	566H	05h	5 MINUTES

Software watchdog timer PET = PORT 566H, write the timeout value.

Standard

The watchdog can be enabled or disabled via software by writing an appropriate timeout value to I/O port 1EEH. See the chart provided below.

Port Address	Value	Reset Interval
1EEH	00h	DISABLED
	01h	3 SECONDS
	03h	30 SECONDS
	05h	300 SECONDS
1EFH	ANY	RESET TIMER

Legacy

The Legacy watchdog timer has a fixed reset interval of 1.5 seconds. The watchdog can be enabled by writing 1 or disabled by writing a 0 to I/O port address 1D0.

Port Address	Value	Reset Interval
1D0H	00h	DISABLED
	01h	Enabled 1.5 sec
1D8H	ANY	RESET TIMER

Real-Time Clock/Calendar

A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be enabled for the real-time clock to retain time and date during a power down.

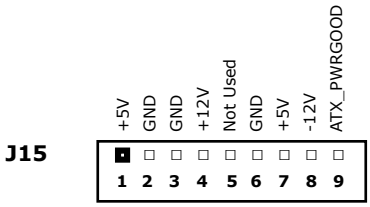
CONNECTOR REFERENCE

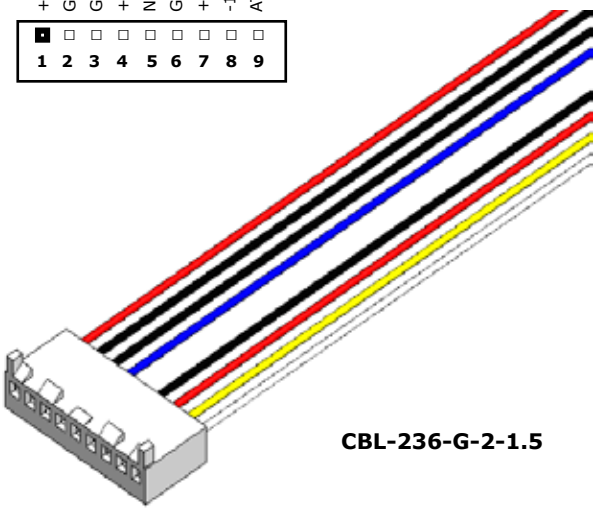
POWER

J15 - Power and Reset

Visual Index

PCB Connector: **MOLEX 26-60-6092 (J15)**
Mating Connector: **MOLEX 09-50-8093 (Housing)**
MOLEX 08-58-0189 (Crimp)





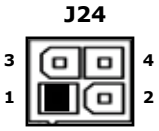
CBL-236-G-2-1.5

Power is applied to the EBC-Z5xx via the connector at **J15**. WinSystems offers the cable CBL-236-G-2-1.5 to simplify this connection.

J24 - ATX Signals

Visual Index

PCB Connector: **MOLEX 46207-1004 (J24)**
Mating Connector: **MOLEX 0039012045 (Housing)**
MOLEX 0039000039 (Crimp)

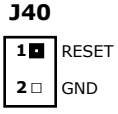


Pin 1	+5VSB
Pin 2	PSON
Pin 3	PWR_BTN
Pin 4	GND

J40 - Push Button Reset

Visual Index

PCB Connector: **MOLEX 22-29-2021 (J40)**
Mating Connector: **MOLEX 10-11-2023 (Housing)**
MOLEX 08-50-0005 (Crimp)



D14 (+5 VSB Power LED), D15 (+5V Power LED)

Visual Index

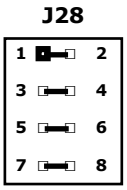
LEDs located at **D14** (+5 VSB Power LED), **D15** (+5V Power LED) indicate the state of the system.

NOTE: D14 and **D15** will always be illuminated during normal operation. When using an ATX power supply and only **D14** is illuminated, the system is in suspend mode.

D14	GREEN	+5VSB
D15	RED	VCC (+5V)

J28 - Power Supply Selection

Visual Index



AT Power	1-2, 3-4, 5-6, 7-8 (default)
ATX Power	1 2, 3 4, 5 6, 7 8

The EBC-Z5xx supports either AT (standard power supply) or ATX type power supplies. Zero load supplies are recommended. **J28** specifies the style of supply connected to the single board computer (SBC). An AT power supply is a simple on/off supply with no interaction with the single board computer. Most embedded systems use this type of power supply and it is the default setting.

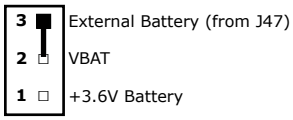
ATX type power supplies function with a “soft” on/off power button and a +5 VSB (standby). If an ATX compatible power supply is connected, **J28** should be set accordingly and a power button (momentary contact) connected between pin 3 (power button) and pin 4 (ground) of **J24**. The +5 VSB signal provides the standby voltage to the EBC-Z5xx but does not power any other features of the board. When the power button is pressed, the EBC-Z5xx pulls PSON (Power Supply On) low and the power supply turns on all voltages to the single board computer. When the power button is pressed again, the BIOS signals the event so ACPI-compliant operating systems can be shutdown before the power is turned off. In ATX mode, if the power button is held for 4 seconds, the power supply is forced off, regardless of ACPI. Since this is software driven, it is possible that a software lockup could prevent the power button from functioning properly. For the BIOS to report the ATX supply to ACPI-compatible operating systems, **J28** must be setup correctly.

BATTERY BACKUP

J43 - Battery Enable/Disable

Visual Index

J43
(Master Battery Enable)



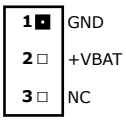
Enables On-board Battery	1-2
Enables External Battery (default)	2-3

J47 - External Battery

Visual Index

PCB Connector: **MOLEX 22-11-2034 (J47)**
Mating Connector: **MOLEX 22-01-3037 (Housing)**
MOLEX 08-55-0102 (Crimp)

J47



(For external battery. Provides battery backup to RTC and BIOS CMOS.)

WARNING: BAT-LTC-E-36-16-1 or BAT-LTC-E-36-27-1 must be connected at J47. Improper installation of the battery could result in explosive failure. Please be careful to note correct connection at location J47.

An optional external battery, connected at **J47**, supplies the EBC-Z5xx board with standby power for the real-time clock and CMOS setup RAM. An extended temperature lithium battery is available from WinSystems, part number BAT-LTC-E-36-16-1 or BAT-LTC-E-36-27-1.

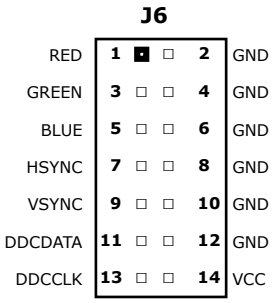
A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the VCC of the systems drops below the battery voltage and back OFF again when VCC returns to normal.

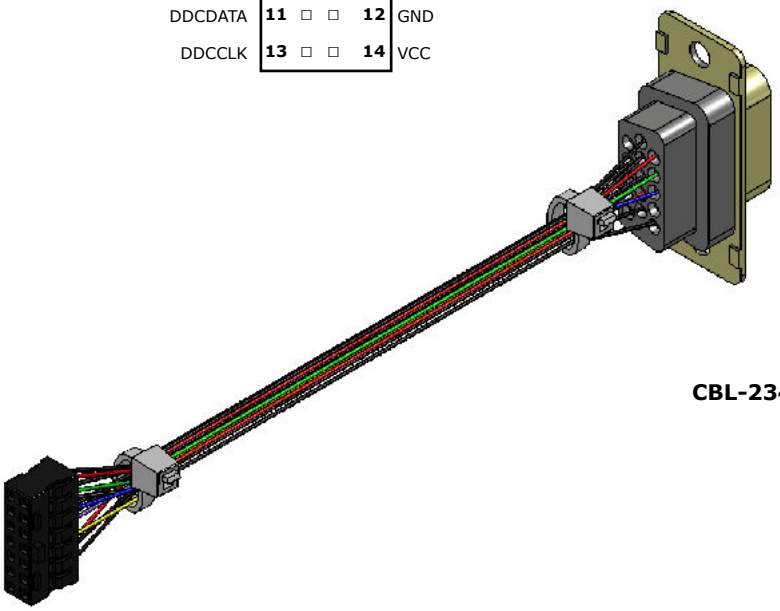
For OEM applications, an on-board battery may be populated. Please contact your WinSystems' Application Engineer for additional information.

J6 - ANALOG VGA

Visual Index

PCB Connector: MOLEX 87832-1420 (J6)
Mating Connector: MOLEX 51110-1451 (Housing)
MOLEX 50394-8051 (Crimp)





CBL-234-G-1-1.375

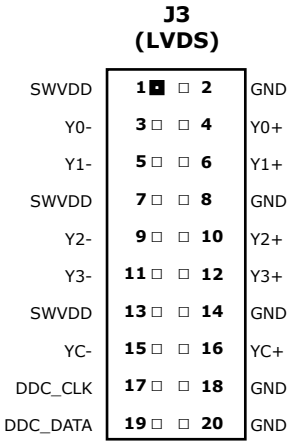
VGA [DB15 Female]

Pin	COLOR	SIGNAL
1	RED	RED
2	GREEN	GREEN
3	BLUE	BLUE
4	-	-
5	BLACK	GND
6	BLACK	GND
7	BLACK	GND
8	BLACK	GND
9	RED	VCC
10	BLACK	GND
11	-	-
12	BLACK	DDCDATA
13	VIOLET	HSYNC
14	YELLOW	VSYNC
15	BLACK	DDCCLK

J3 - LVDS

Visual Index

PCB Connector: MOLEX 87832-2020 (J3)
Mating Connector: MOLEX 51110-2051 (Housing)
MOLEX 50394-8100 (Crimp)

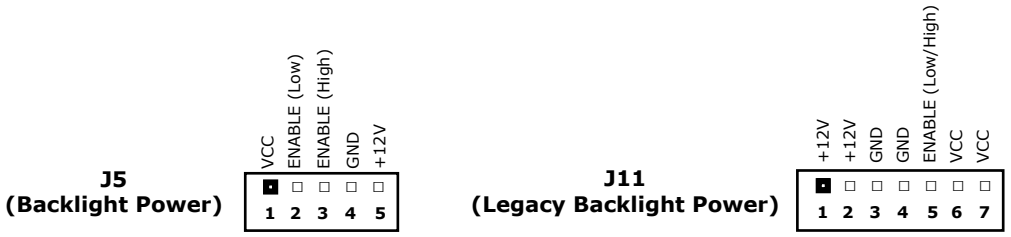


J5, J11 - Backlight Power

Visual Index

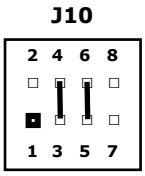
PCB Connector: MOLEX 53398-0571 (J5)
Mating Connector: MOLEX 51021-0500 (Housing)
MOLEX 50079-8100 (Crimp)

PCB Connector: MOLEX 22-11-2072 (J11)
Mating Connector: MOLEX 22-01-2077 (Housing)
MOLEX 08-55-0102 (Crimp)



HAZARD WARNING: **LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring and handling the inverter output. To avoid the danger of shock and to avoid the panel, make all connection changes with the power removed.**

J10 - Panel Options



Panel Power	5V 3.3V (default)	1-2, 3 4 1 2, 3-4
Backlight Enable for J11	Active High Enable (default) Active Low Enable	5-6, 7 8 5 6, 7-8

Avoid Simultaneous Jumpering of pins 1-2 and 3-4.
Misjumpering panel power causes damage to the board and/or the Flat Panel.

The EBC-Z5xx has an integrated display controller that interfaces to both Analog VGA and flat panel displays. The video output mode is selected in the CMOS setup. Simultaneous flat panel and Analog VGA mode is also supported. The Analog VGA connector is located at **J6**. WinSystems offers the cable CBL-234-G-1-1.375 to simplify the connection. The LVDS interface connector is located at **J3** to interface to flat panels. Two backlight power connectors are located at **J5** and **J11**. Panel power option selection is made at **J10**.

When using 800x600 resolution in DOS environment, VESA mode 103 is not supported.

Contact your WinSystems' Applications Engineer for information about available cable kits and supported panels.
This manual does not attempt to provide any information about how to connect to specific LCDs.

J2 - 5.1 Audio

Visual Index

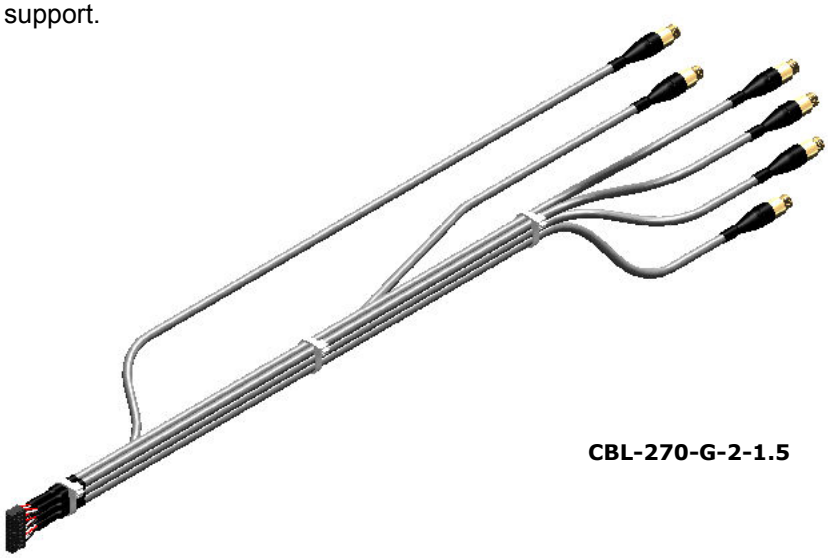
PCB Connector: MOLEX 87832-1820 (J2)
Mating Connector: MOLEX 51110-1851 (Housing)
MOLEX 50394-8100 (Crimp)

J2

OUT-R	1	2	MIC1-REAR-R
OUT-L	3	4	MIC1-REAR-L
ADGND	5	6	ADGND
SUR-R	7	8	MIC2-FRONT-R
SUR-L	9	10	MIC2-FRONT-L
ADGND	11	12	ADGND
CENTER	13	14	LINE_R
LFE	15	16	LINE_L
ADGND	17	18	ADGND

Audio External Connection

Audio connection is provided at **J2**. Two cables are available from WinSystems to adapt to this connector. CBL-270-G-2-1.5 provides full 5.1 audio support. A simplified cable, CBL-270-G-2-1.5, provides basic Line In, Line Out, and Microphone audio support.

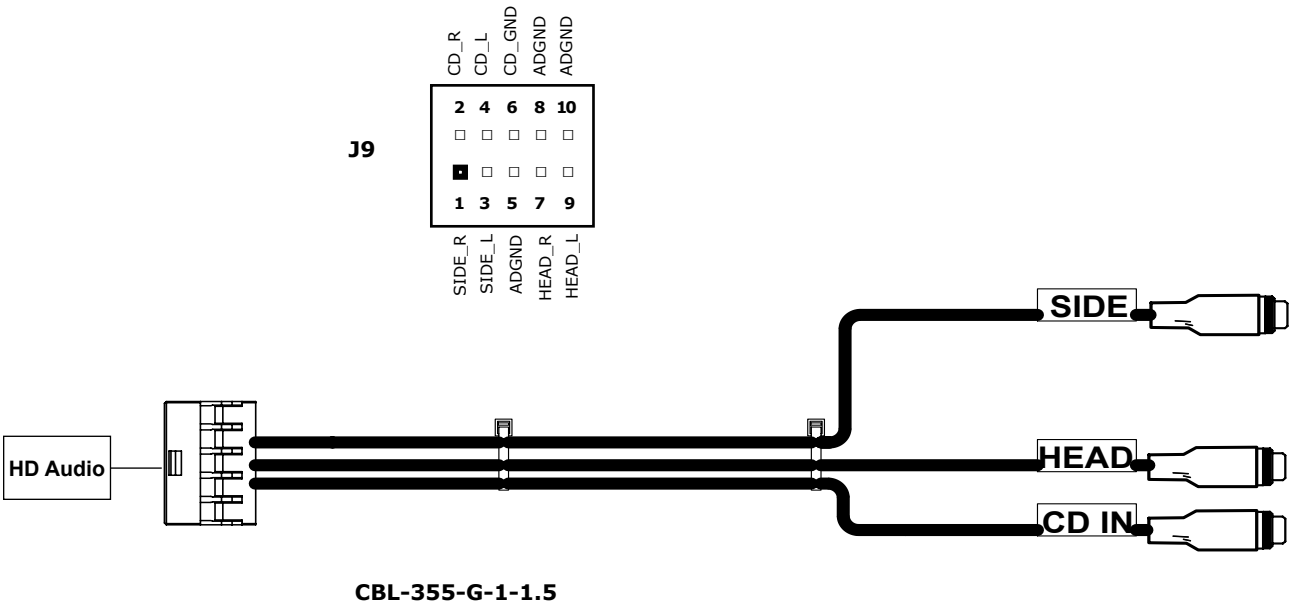


CBL-270-G-2-1.5

CBL-270-G-3-1.5

J9 - HD Audio Extension

PCB Connector: **MOLEX 87832-1006 (J9)**
Mating Connector: **MOLEX 51110-1060 (Housing)**
MOLEX 50394-8100 (Crimp)



CBL-355-G-1-1.5

HD audio extension is provided at **J9.** **J9** extends 5.1 to achieve a full 7.1 surround in conjunction with CBL-270-G-2-1.5 at **J2**. This connector also provides CD-Input and Headphone connectivity.

SP1 - Speaker

Speaker

An on-board speaker, **SP1**, is available for sound generation.

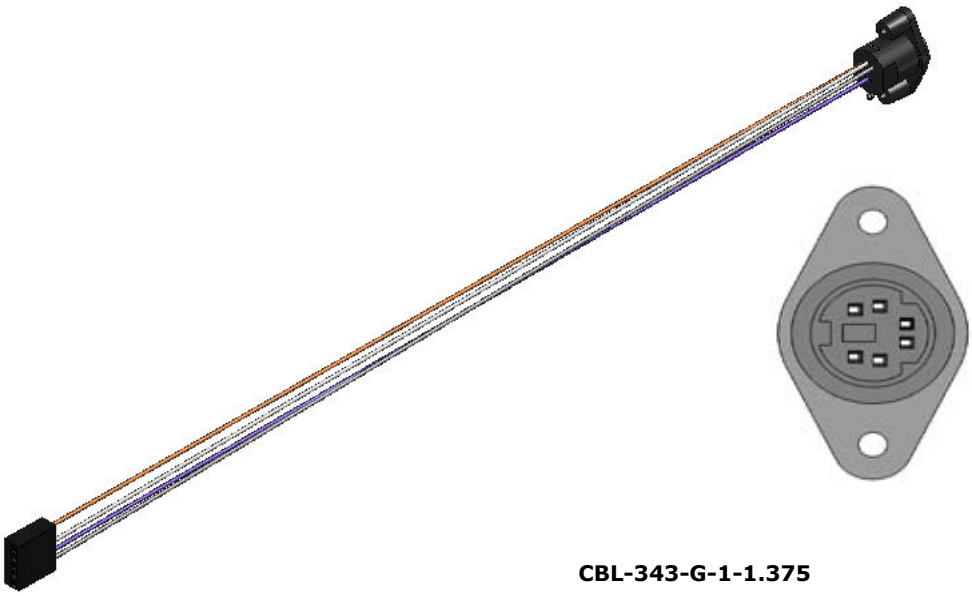
Beep Codes

Reference the chart Appendix-B section of this manual for the appropriate beep codes.

J13 - Mouse

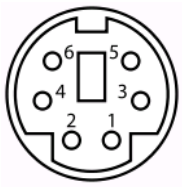
Visual Index

PCB Connector: **MOLEX 22-11-2052 (J13)**
Mating Connector: **MOLEX 22-01-3057 (Housing)**
MOLEX 08-55-0102 (Crimp)



CBL-343-G-1-1.375

PS/2 Mouse [6-Position]



Pin	Description
1	MSDATA
2	NC
3	GND
4	VCC
5	MSCLK
6	N/C

A PS/2 mouse port provides connection for a compatible mouse and is terminated at **J13**. An adapter cable, CBL-343-G-1-1.375, is available from WinSystems to simplify the connection. Optionally, a USB mouse can be connected in addition to, or instead of the standard PS/2 mouse. The pinout for the cable is listed above.

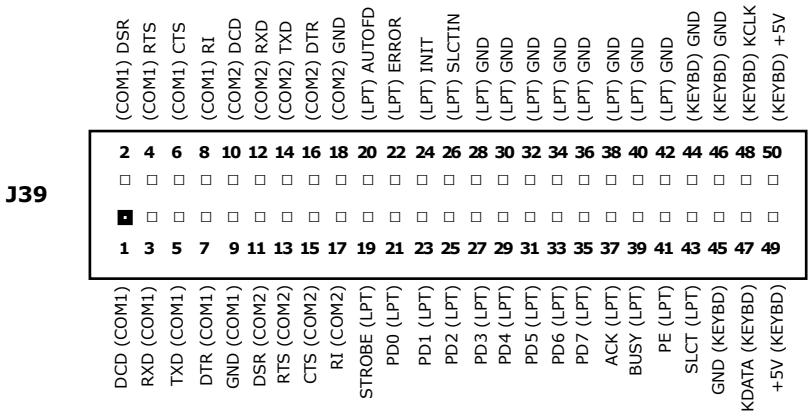
J39 - Multi-I/O (COM1, COM2, Keyboard, LPT)

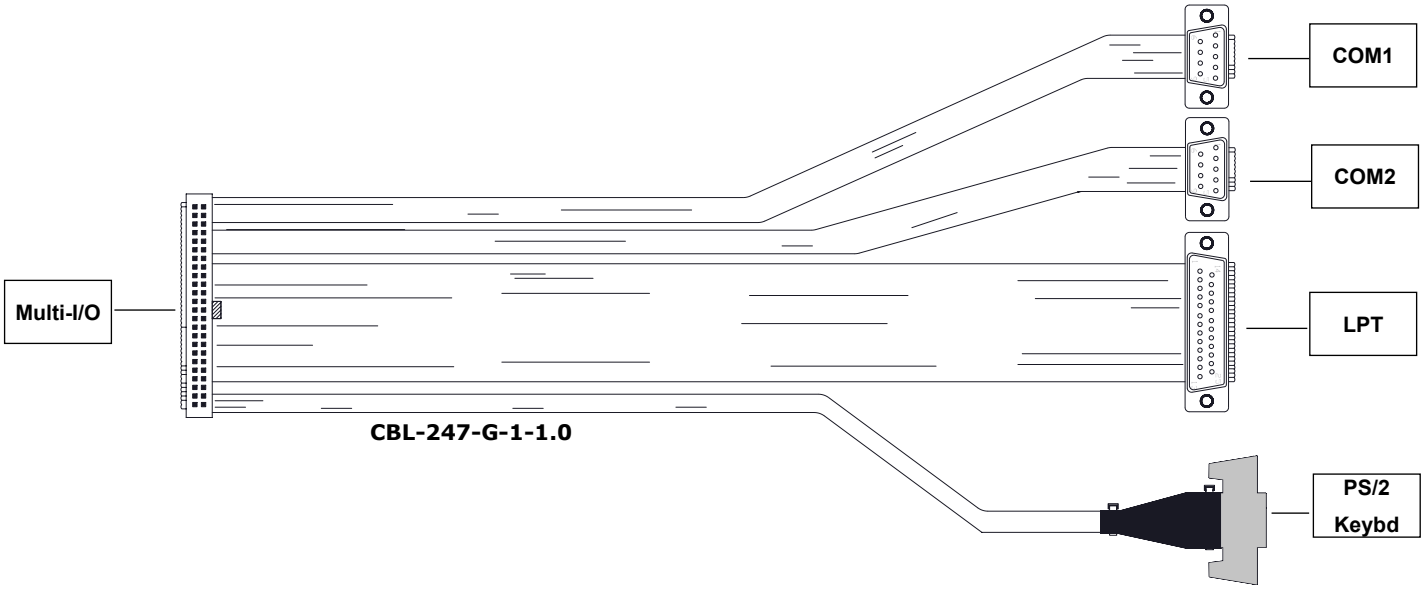
Visual Index

PCB Connector: **TEKA SVC225C405M123-0 (J39)**

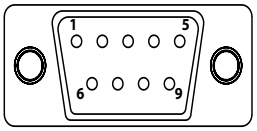
Mating Connector: **ITW-PANCON 050-050-455A**

The interface to I/O serial ports (COM1/COM2), the printer port and keyboard are all terminated via the connector at **J39**. A cable, part number CBL-247-G-1-1.0, is available from WinSystems to adapt to the conventional I/O connectors. The pinout definition for **J39** is listed below.





COM1, COM2 [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

All serial ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 transceivers have charge pumps to generate the plus and minus voltages so the EBC-Z5xx only requires +5V to operate.

Each port is setup to provide internal diagnostics such as loopback and echo mode on the data stream. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

COM1 and COM2 Configuration Options in BIOS

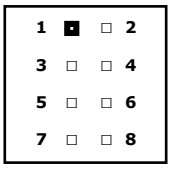
1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Mode(s)	Configuration Note
2, 4, 5	Require the RTS bit (MCR Bit 1) to be set in order to transmit.
3, 6, 7	Require TX/RX(300) termination on one node.
4	Requires the RTS (MCR Bit 1) be de-asserted in order to receive.
* Each of the RS-422/RS-485 modes allow for jumper selection of transmit and/or receive termination and biasing resistor(s). An 8-pin configuration jumper is provided for each port.	

Termination Resistors

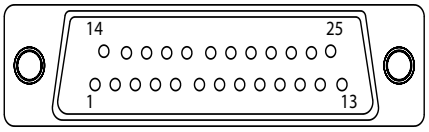
COM1 = **J36**

COM2 = **J42**



RS-422/RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		3-4
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	1-2
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	3-4
	Places a 100Ω Resistor from Ground to TX/RX-	5-6

LPT [DB25 Female]

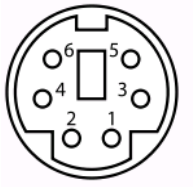


Pin	SPP Signal
1	STROBE
2-9	PD0-PD7
10	ACK
11	BUSY
12	PE
13	SLCT
14	AUTOFD
15	ERROR
16	INIT
17	SLCTIN
18-25	GND

The LPT port is a multimode parallel printer port that supports the PS/2 Standard Bidirectional Parallel Port (SPP) and Enhanced Parallel Port (EPP) functionality. The output drivers support 8 mA per line.

The printer port can also be used as two additional general-purpose I/O ports if a printer is not required. The first port is configured as eight input or output only lines. The other port is configured as five input and three output lines.

PS/2 Keyboard [6-Position]



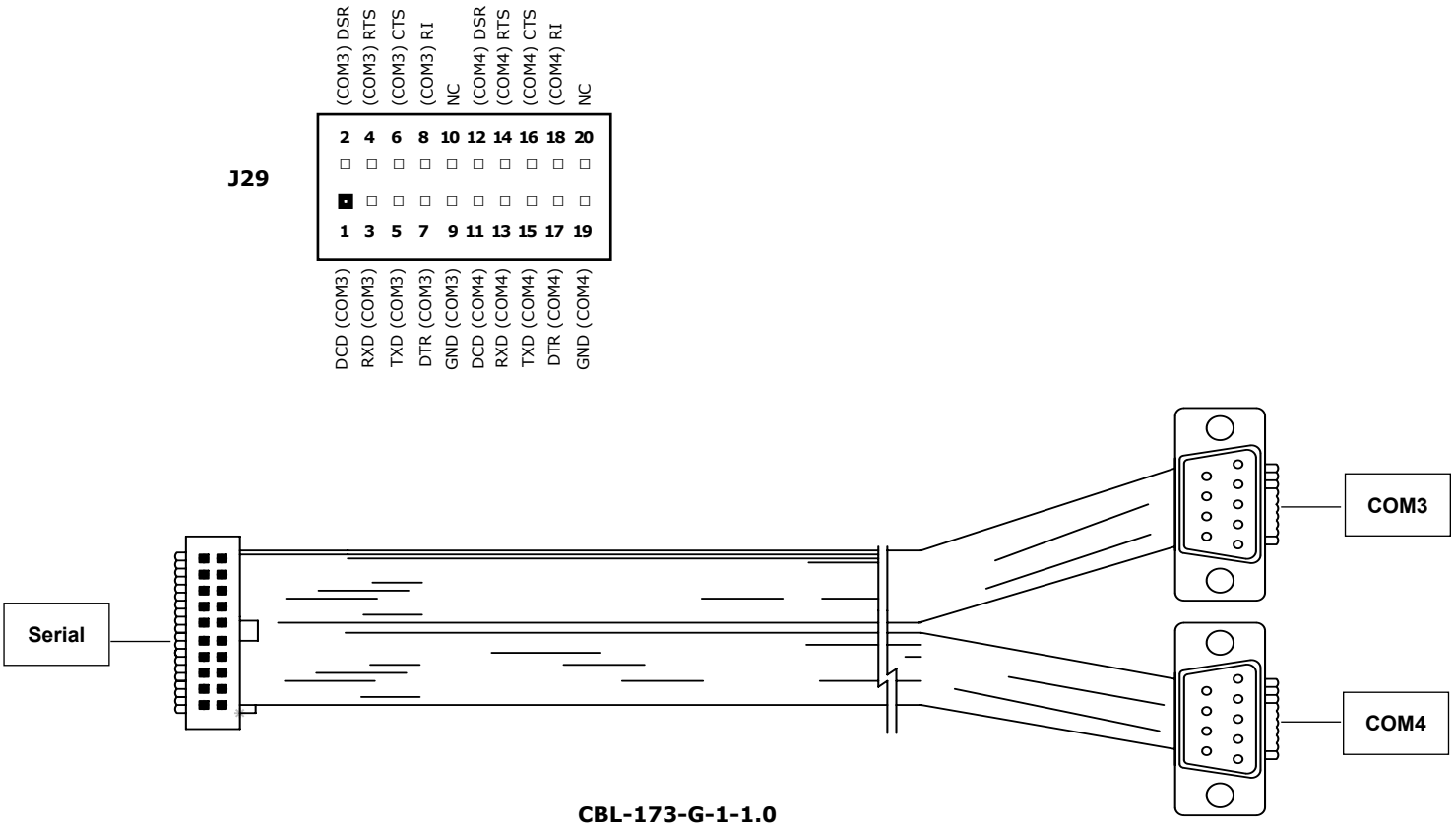
Pin	Description
1	KDATA
2	NC
3	GND
4	+5V
5	KCLK
6	NC

This connector supports a PS/2 keyboard interface. The pinout for the cable is listed above.

J29 - COM3, COM4

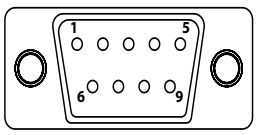
Visual Index

PCB Connector: **TEKA SVC210C405M123-0 (J29)**
Mating Connector: **ITWPANCON 050-020-455A**



CBL-173-G-1-1.0

COM3, COM4 [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

Both ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 has a charge pump to generate the plus and minus voltages so the EBC-Z5xx only requires +5V to operate. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

COM3 and COM4 Configuration Options in BIOS

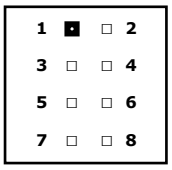
1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Mode(s)	Configuration Note
2, 4, 5	Require the RTS bit (MCR Bit 1) to be set in order to transmit.
3, 6, 7	Require TX/RX(300) termination on one node.
4	Requires the RTS (MCR Bit 1) be de-asserted in order to receive.
* Each of the RS-422/RS-485 modes allow for jumper selection of transmit and/or receive termination and biasing resistor(s). An 8-pin configuration jumper is provided for each port.	

Termination Resistors

COM3 = **J31**

COM4 = **J32**

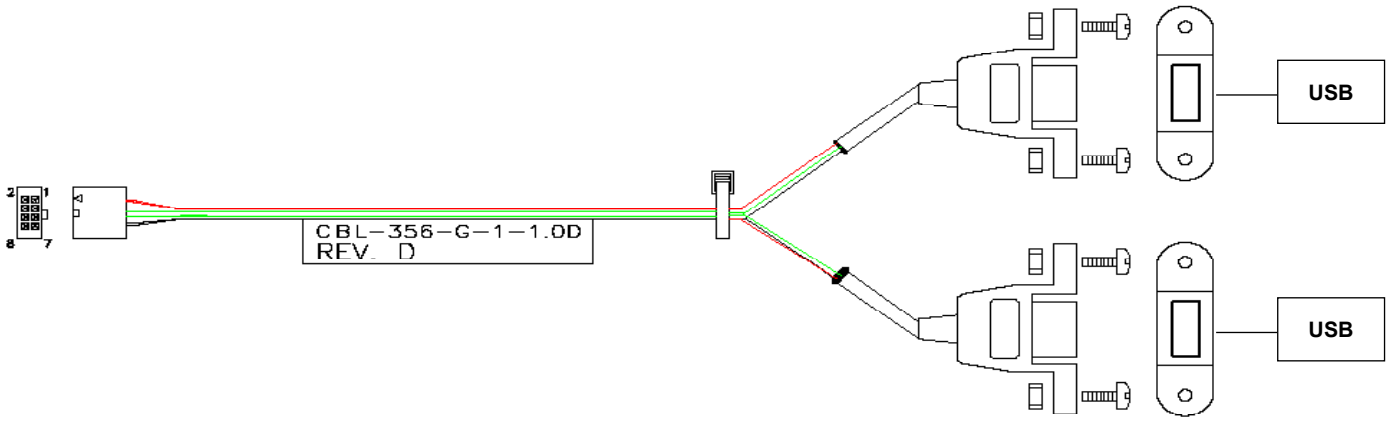


RS-422/RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		3-4
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	1-2
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	3-4
	Places a 100Ω Resistor from Ground to TX/RX-	5-6

J35, J46 - USB

Visual Index

PCB Connector: MOLEX 87832-0806 (J35, J46)
Mating Connector: MOLEX 51110-0860 (Housing)
MOLEX 50394-8051 (Crimp)



CBL-356-G-1-1.0

Up to two USB cables may be attached to the EBC-Z5xx via the connectors for a total of four USB 2.0 ports. These are terminated to an 8-pin, 2 mm connector at **J35** and **J46**. An adapter cable CBL-356-G-1-1.0 is available from WinSystems for connection.

Two additional USB ports are available for expansion on the SUMIT™ interface.

USB Power LED	
LED	**Port**
D9	USB1
D10	USB0
D11	USB3
D12	USB2

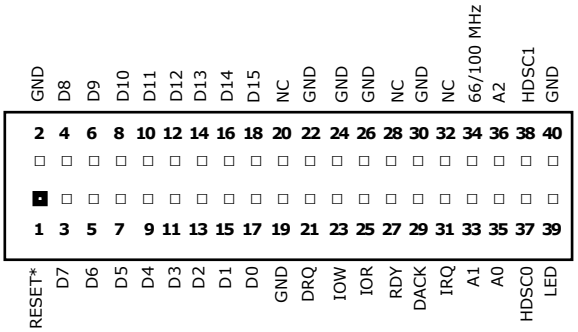
PARALLEL ATA

J22, J23 - PATA

Visual Index

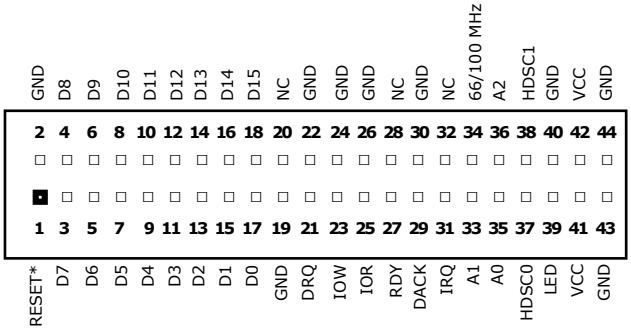
PCB Connector: **TEKA SVC220C405M123-0 (J22)**
Mating Connector: **CIRCUIT ASSEMBLY CA-40ATAS-C**

J22



PCB Connector: **SAMTEC STMM-122-02-G-D-SM-P-TR (J23)**
Mating Connector: **SAMTEC ASP-129789-01**

J23



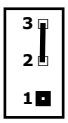
The EBC-Z5xx supports the PATA interface at **J22** (40-pin primary) and **J23** (44-pin primary).

COMPACTFLASH

J44 - COMPACTFLASH

Visual Index

J41



CompactFlash Master	1-2
CompactFlash Slave (default)	2-3

When using a CompactFlash device, Master/Slave selection is made using jumper field **J41**. The EBC-Z5xx supports solid state CompactFlash storage devices for applications where the environment is too harsh for mechanical hard disks.

The CompactFlash socket at **J44** supports modules with TrueIDE support. WinSystems offers industrial grade CompactFlash modules that provide high performance and extended temperature operation (-40ºC to +85ºC). A PATA activity LED is present at **D13**.

The CompactFlash is an PATA device. Use of a CompactFlash device therefore reduces the number of available PATA devices to one.

J7, J8 - Gigabit Ethernet

Visual Index

PCB Connector: **TYCO 5556416-1 (J7, J8)**

PC82573L Gigabit Ethernet Controllers

The EBC-Z5xx is equipped with two Intel PC82573L Gigabit Ethernet controllers. Each of these provides a standard IEEE 802.3 Ethernet interface for 1000/100/10BASE-T networks. The RJ-45 connections for each Ethernet port are available at **J7** (Port 1) and **J8** (Port 2).

On-board Ethernet activity LEDs **D1-D3** are provided for Port 1. LEDs **D6-D8** are associated with Port 2. These activity signals are also available off-board for enclosures or other applications that have remote mounting requirements. The activity signals for Port 1 are provided at connector **J1**. The signals for Port 2 are provided at **J14**. See tables below for signal and pin definitions.

J1
(Ethernet Port 1)

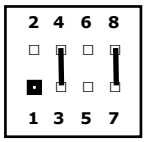
Pin	LED	Color	Signal
1	D1	GREEN	ACTIVITY
2	-	-	+3VSB
3	D2	RED	SPEED100
4	-	-	+3VSB
5	D3	RED	SPEED1000
6	-	-	+3VSB

J14
(Ethernet Port 2)

Pin	LED	Color	Signal
1	D6	GREEN	ACTIVITY_A
2	-	-	+3V
3	D7	RED	SPEED100_A
4	-	-	+3V
5	D8	RED	SPEED1000_A
6	-	-	+3V

J12 - Ethernet Configuration

J12



Ethernet Port 1	
Non-Volatile Memory Protection (Install Jumper to Disable Protection)	1-2
Auxiliary Power Present (Remove Jumper when powered in ATX Mode - Default Installed)	3-4
Ethernet Port 2	
Non-Volatile Memory Protection (Install Jumper to Disable Protection)	5-6
Ethernet Port 2 Present (If Ethernet Port 2 is not installed, remove jumper)	7-8

D16 - Status LED

Visual Index

A status LED is populated on the board at **D16** which can be used for any application specific purpose. The LED can be turned on in software applications by writing a **1** to I/O port 1EDH. The LED can be turned off by writing a **0** to 1EDH.

D16	--	GREEN	STATUS

J37, J38 - Digital I/O

Visual Index

PCB Connector: TEKA SVC225C405M123-0 (J37, J38)
Mating Connector: ITW-PANCON 050-050-455A

J37 (Ports 0/1/2)

GND	50	49	+5V
GND	48	47	Port 0 Bit 0
GND	46	45	Port 0 Bit 1
GND	44	43	Port 0 Bit 2
GND	42	41	Port 0 Bit 3
GND	40	39	Port 0 Bit 4
GND	38	37	Port 0 Bit 5
GND	36	35	Port 0 Bit 6
GND	34	33	Port 0 Bit 7
GND	32	31	Port 1 Bit 0
GND	30	29	Port 1 Bit 1
GND	28	27	Port 1 Bit 2
GND	26	25	Port 1 Bit 3
GND	24	23	Port 1 Bit 4
GND	22	21	Port 1 Bit 5
GND	20	19	Port 1 Bit 6
GND	18	17	Port 1 Bit 7
GND	16	15	Port 2 Bit 0
GND	14	13	Port 2 Bit 1
GND	12	11	Port 2 Bit 2
GND	10	9	Port 2 Bit 3
GND	8	7	Port 2 Bit 4
GND	6	5	Port 2 Bit 5
GND	4	3	Port 2 Bit 6
GND	2	1	Port 2 Bit 7

J38 (Ports 3/4/5)

GND	50	49	+5V
GND	48	47	Port 3 Bit 0
GND	46	45	Port 3 Bit 1
GND	44	43	Port 3 Bit 2
GND	42	41	Port 3 Bit 3
GND	40	39	Port 3 Bit 4
GND	38	37	Port 3 Bit 5
GND	36	35	Port 3 Bit 6
GND	34	33	Port 3 Bit 7
GND	32	31	Port 4 Bit 0
GND	30	29	Port 4 Bit 1
GND	28	27	Port 4 Bit 2
GND	26	25	Port 4 Bit 3
GND	24	23	Port 4 Bit 4
GND	22	21	Port 4 Bit 5
GND	20	19	Port 4 Bit 6
GND	18	17	Port 4 Bit 7
GND	16	15	Port 5 Bit 0
GND	14	13	Port 5 Bit 1
GND	12	11	Port 5 Bit 2
GND	10	9	Port 5 Bit 3
GND	8	7	Port 5 Bit 4
GND	6	5	Port 5 Bit 5
GND	4	3	Port 5 Bit 6
GND	2	1	Port 5 Bit 7

The EBC-Z5xx has 48 open collector digital I/O bits with a default base address of 120H. Each bit is configured as an open collector with a 10K pullup. Each bit is able to sink up to 12mA. The first 24 lines are capable of fully latched event sensing with polarity being software programmable.

Digital I/O Connectors

These 48 lines of digital I/O are terminated through two 50-pin connectors at **J37** and **J38**. The **J37** connector handles I/O ports 0 through 2 while **J38** handles ports 3 through 5.

J50 - Digital I/O Power

Visual Index

The I/O connectors can provide +5V or +3.3V to an I/O rack for miscellaneous purposes by jumpering **J50**. When **J50** is jumpered (1-2), +5V is provided at pin 49 of **J37** and **J38**. If **J50** is jumpered (3-4), then +3.3V is provided at pin 49 of **J37** and **J38**. It is the user's responsibility to limit current to a safe value (less than 400 mA) to avoid damaging the CPU board.

J50

3	4
1	2

STOP

Avoid Simultaneous Jumpering of pins 1-2 and 3-4.
Misjumpering causes damage to the board.

+3.3V is provided at pin 49 of **J37/J38**	3-4
+5V is provided at pin 49 of **J37/J38**	1-2
No Power at Pin 49 of **J37/J38** (default)	1 2, 3 4

Register Definitions (WS16C48)

The EBC-Z5xx uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers, and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01H	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02H	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03H	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04H	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05H	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06H	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07H	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08H	Reserved	Pol_0	Enab_0	Int_ID0
09H	Reserved	Pol_1	Enab_1	Int_ID1
0AH	Reserved	Pol_2	Enab_2	Int_ID2

Register Details

Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK

This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A **1** written to the I/O port position will prohibit further writes to the corresponding I/O port.

POL0 - POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

ENAB0 - ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

INT_ID0 – INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

J45, J48 - PC/104

Visual Index

PCB Connector: **TEKA PC232-A-1BD-M (J45)**
TEKA PC220-A-1BD-M (J48)

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on EBC-Z5xx's connectors, located at **J45** and **J48**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J48 (C/D)

GND	D0	C0		GND
MEMCS16#	D1	C1		SBHE#
IOCS16#	D2	C2		LA23
IRQ10	D3	C3		LA22
IRQ11	D4	C4		LA21
IRQ12	D5	C5		LA20
IRQ15	D6	C6		LA19
IRQ14	D7	C7		LA18
DACK0#	D8	C8		LA17
DRQ0	D9	C9		MEMR#
DACK5#	D10	C10		MEMW#
DRQ5	D11	C11		SD8
DACK6#	D12	C12		SB9
DRQ6	D13	C13		SD10
DACK7#	D14	C14		SD11
DRQ7	D15	C15		SD12
+5V	D16	C16		SD13
MASTER#	D17	C17		SD14
GND	D18	C18		SD15
GND	D19	C19		KEY

J45 (A/B)

IOCHK#	A1	B1		GND
SD7	A2	B2		RESET
SD6	A3	B3		+5V
SD5	A4	B4		IRQ
SD4	A5	B5		-5V
SD3	A6	B6		DRQ2
SD2	A7	B7		-12V
SD1	A8	B8		SRDY#
SD0	A9	B9		+12V
IOCHRDY	A10	B10		KEY
AEN	A11	B11		SMEMW#
SA19	A12	B12		SMEMR#
SA18	A13	B13		IOW#
SA17	A14	B14		IOR#
SA16	A15	B15		DACK3#
SA15	A16	B16		DRQ3
SA14	A17	B17		DACK1#
SA13	A18	B18		DRQ1
SA12	A19	B19		REFRESH#
SA11	A20	B20		BCLK
SA10	A21	B21		IRQ7
SA9	A22	B22		IRQ6
SA8	A23	B23		IRQ5
SA7	A24	B24		IRQ4
SA6	A25	B25		IRQ3
SA5	A26	B26		DACK2#
SA4	A27	B27		TC
SA3	A28	B28		BALE
SA2	A29	B29		+5V
SA1	A30	B30		OSC
SA0	A31	B31		GND
GND	A32	B32		GND

= Active Low Signal

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

J26, J27 - SUMIT

Visual Index

PCB Connector: **SAMTEC ASP-129637-01 (J26, J27)**

J27 (SUMIT-A)

5V	1	2	12V
3.3V_1	3	4	SMB_DATA
3.3V_2	5	6	SMB_CLK
EXPCD_REQ#	7	8	SMB_ALERT
EXPCD_PRSNT#	9	10	SPI_DO
USB_OC#0/1	11	12	SPI_DI
USB_OC#0/1	13	14	SPI_CLK
5V_2	15	16	SPI_CS0
USB3+	17	18	SPI_CS1
USB3-	19	20	RESERVED_5
5V_3	21	22	LPC_DRQ
USB2+	23	24	LPC_AD0
USB2-	25	26	LPC_AD1
5V_4	27	28	LPC_AD2
USB1+	29	30	LPC_AD3
USB1-	31	32	LPC_FRAME#
5V_5	33	34	SERIRQ#
USB0+	35	36	LPC_PRSNT#/GND
USB0-	37	38	CLK_33MHz
GND_1	39	40	GND_3
A_PETp0	41	42	A_PERp0
A_PETn0	43	44	A_PERn0
GND_2	45	46	APRSNT
PERST#	47	48	A_CLKp
WAKE#	49	50	A_CLKn
5V_6	51	52	GND_4

J26 (SUMIT-B)

5V	1	2	GND
B_PETp0	3	4	B_PERp0
B_PETn0	5	6	B_PERn0
GND	7	8	BPRST#/GND
C_CLKp	9	10	B_CLKp
C_CLKn	11	12	B_CLKn
CPRSNT#/GND	13	14	GND
C_PETp0	15	16	C_PERp0
C_PETn0	17	18	C_PERn0
GND_2	19	20	GND
C_PETp1	21	22	C_PERp1
C_PETn1	23	24	C_PERn1
GND	25	26	GND
C_PETp2	27	28	C_PERp2
C_PETn2	29	30	C_PERn2
GND_3	31	32	GND
C_PETp3	33	34	C_PERp3
C_PETn3	35	36	C_PERn3
GND_4	37	38	GND
PERST#	39	40	WAKE#
RESERVED	41	42	RESERVED
5V_2	43	44	RESERVED
RV_3	45	46	3.3V
5V_4	47	48	3.3V_2
5V_5	49	50	3.3V_3
5V_6	51	52	5V_7

The EBC-Z5xx has a SUMIT-A connector which allows for multiple I/O modules to be stacked on top of a host module. The SUMIT-A connector is located at **J27**. A second SUMIT-B connector is located at **J26**. The pinouts for **J27** and **J26** are listed above. Refer to the SUMIT Specification for more information on SUMIT.

MiniPCI EXPRESS

J102 - MiniPCIe

Visual Index

PCB Connector: **MOLEX 0679105700 (J102)**

The EBC-Z5xx includes a MiniPCIe socket at **J102**. Though the socket can support other devices, it is most often used to add wireless Ethernet cards from Broadcom®, Foxconn®, (Atheros), or others.

NOTE: Intel® boards are not supported by the EBC-Z5xx.

Pin	Name	Pin	Name
2	3.3Vaux	**1**	WAKE#
4	GND	**3**	COEX1
6	1.5V	**5**	COEX2
8	UIM_PWR	**7**	CLKREQ#
10	UIM_DATA	**9**	GND
12	UIM_CLK	**11**	REFCLK-
14	UIM_RESET	**13**	REFCLK+
16	UIM_VPP	**15**	GND
Mechanical Key			
18	GND	**17**	Reserved (UIM_C8)
20	W_DISABLE#	**19**	Reserved (UIM_C4)
22	PERST#	**21**	GND
24	+3.3Vaux	**23**	PERn0
26	GND	**25**	PERp0
28	+1.5V	**27**	GND
30	SMB_CLK	**29**	GND
32	SMB_DATA	**31**	PETn0
34	GND	**33**	PETp0
36	USB_D-	**35**	GND
38	USB_D+	**37**	GND
40	GND	**39**	+3.3Vaux
42	LED_WWAN#	**41**	+3.3Vaux
44	LED_WLAN#	**43**	GND
46	LED_WPAN#	**45**	Reserved
48	+1.5V	**47**	Reserved
50	GND	**49**	Reserved
52	+3.3Vaux	**51**	Reserved

J101 - MiniPCIe Antenna Passthrough Connnection

Visual Index

PCB Connector: **SAMTEC ASP-129637-01 (J101)**

J19 - MiniPCIe Antenna

Visual Index

PCB Connector: **SAMTEC RSP-14946 (J19)**
SAMTEC RSP-14946-01 (J19)

J53 - SIM Card Socket

Visual Index

Some MiniPCIe cards may require external SIM cards. The external SIM card may be added at **J53**.

General Information

The EBC-Z5xx includes BIOS from Phoenix Technologies to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the BIOS Settings Storage Options section of this manual. Access to this setup information is via the Setup Utility in the BIOS.

Entering Setup

To enter setup, power up the computer and press **F2** when either the splash screen is displayed or when the **Press F2 for Setup** message is displayed. It may take a few seconds before the main setup menu screen is displayed.

Navigation of the Menus

Use the **Up** and **Down** arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. Following are images of each menu screen in the default configuration along with a brief description of each option where applicable. Available options are listed in reference tables. Menu values shown in **bold** typeface are factory defaults.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Main Menu	
System Time:	**09:40:34**
System Date:	**06/20/2009**
Large Disk Access Mode:	**DOS**
Options: Other DOS	
> Primary Master	**None**
> Primary Slave	**None**
System Memory:	640 KB
Extended Memory:	502 MB
Ethernet MAC Address 1:	xx:xx:xx:xx:xx:xx
Ethernet MAC Address 2:	xx:xx:xx:xx:xx:xx
CPU Temperature:	50 °C/122 °F

Each available option is listed in detail in the following sections.

Navigation to the screens is located at the top of each screen's layout.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **Primary Master/Slave (Type: Auto)**	
Type:	**Auto**
Options: None ATAPI Removable CD-ROM IDE Removable Other ATAPI User Auto	
	CHS Format
Cylinders:	1003
Heads:	16
Sectors:	32
Maximum Capacity:	263 MB
	LBA Format
Total Sectors:	513536
Maximum Capacity:	263 MB
Multi-Sector Transfers:	Disabled
LBA Mode Control:	Enabled
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	FPIO 4 / DMA 2
Ultra DMA Mode:	Disabled

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **Primary Master/Slave (Type: None)**	
Type:	**None**
Options: None ATAPI Removable CD-ROM IDE Removable Other ATAPI User Auto	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **Primary Master/Slave (Types: ATAPI Removable, CD-ROM, IDE Removable, Other ATAPI)**	
Type:	**ATAPI Removable** or **CD-ROM** or **IDE Removable**, or **Other ATAPI**
Options: None ATAPI Removable CD-ROM IDE Removable Other ATAPI User Auto	
Multi-Sector Transfers:	**Disabled**
Options: Disabled 2 Sectors 4 Sectors 8 Sectors 16 Sectors	
LBA Mode Control:	**Disabled**
Options: Disabled Enabled	
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**Standard**
Options: Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	
Ultra DMA Mode:	**Disabled**
Options: Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **Primary Master/Slave (Type: User)**	
Type:	**User**
Options: None ATAPI Removable CD-ROM IDE Removable Other ATAPI User Auto	
	CHS Format
Cylinders:	**1003**
Options: 1003 - 1023	
Heads:	**16**
Options: 1-16	
Sectors:	**32**
Options: 0-32	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **Primary Master/Slave (Type: User)** (continued)	
Maximum Capacity:	**263 MB** ***Values may vary based on changes to Cylinders, Heads, or Sectors options**
	LBA Format
Total Sectors:	**513536**
Maximum Capacity:	**263 MB**
Multi-Sector Transfers:	**Disabled**
Options: Disabled 2 Sectors 4 Sectors 8 Sectors 16 Sectors	
LBA Mode Control:	**Enabled**
Options: Disabled Enabled	
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**FPIO 4 / DMA 2**
Options: Standard Fast PIO 1 Fast PIO 2 Fast PIO3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	
Ultra DMA Mode:	**Disabled**
Options: Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced	
Installed O/S:	**WinXP**
Options: Other Win95 Win98 WinMe Win2000 WinXP	
Reset Configuration Data:	**No**
Options: No Yes	
> Keyboard Features	
PS/2 Mouse:	**Auto Detect**
Options: Disabled Enabled Auto Detect	
Summary screen:	**Disabled**
Options: Disabled Enabled	
Boot-time Diagnostic Screen:	**Disabled**
Options: Disabled Enabled	
QuickBoot Mode:	**Enabled**
Options: Disabled Enabled	
Extended Memory Testing:	**None**
Options: Normal Just zero it None	
PXE Option ROM:	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > **Keyboard Features**	
Numlock:	**On**
Options: Auto On Off	
Key Click:	**Disabled**
Options: Disabled Enabled	
Keyboard auto-repeat rate:	**30/sec**
Options: 30/sec 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	
Keyboard auto-repeat delay:	**1/2 sec**
Options: 1/4 sec 1/2 sec 3/4 sec 1 sec	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel
> Atom CPU Control Sub-Menu
> SCH Control Sub-Menu
> Video (Intel IGD) Control Sub-Menu
> Super I/O Control Sub-Menu
> ACPI Control Sub-Menu

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **Atom CPU Control Sub-Menu**	
Hyperthreading:	**Enabled**
Options: Disabled Enabled	
Processor Power Management:	**Enabled**
Options: Disabled GV3 Only C-States Only Enabled	
Enhanced C-States Enable:	**Enabled**
Options: Disabled Enabled	
Timestamp Counter Updates	**Enabled**
Options: Disabled Enabled	
> CPU Thermal Control Sub-Menu	
Set Max Ext CPUID = 3	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Atom CPU Control Sub-Menu > **CPU Thermal Control Sub-Menu**	
Thermal Control Circuit:	**TM1 and TM2**
Options: Disabled TM1 TM2 TM1 and TM2	
PROCHOT# Enable:	**Disabled**
Options: Disabled Enabled	
DTS Enable:	**Enabled**
Options: Disabled Enabled	
Passive Cooling Trip Point:	**79 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive TC1 Value:	**1**
Passive TC2 Value:	**5**
Options: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
More CPU Thermal Control Sub-Menu options are continued on the next page.	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Atom CPU Control Sub-Menu > CPU Thermal Control Sub-Menu (continued)

Passive TSP Value:	**10**

Options:
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150

Critical Trip Point:	**POR**

Options:
POR
71 C
79 C
87 C
95 C
103 C
111 C
119 C

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **SCH Control Sub-Menu**	
> PCI Express Control Sub-Menu	
> SCH USB Control Sub-Menu	
Azalia - Device 27, Function 0:	**Auto**
Options: Disabled Auto	
SDIO - Device 30, Function 0/1/2:	**Enabled**
Options: Disabled Enabled	
Serial IRQ Quiet Mode:	**Enabled**
Options: Disabled Enabled	
Pop Up Mode Enable:	**Enabled**
Options: Disabled Enabled	
Pop Down Mode Enable:	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > SCH Control Sub-Menu > **PCI Express Control Sub-Menu**	
PCI Express - Root Port 1:	**Auto**
Options: Disabled Enabled Auto	
PCI Express - Root Port 2:	**Auto**
Options: Disabled Enabled Auto	
Root Port ASPM Support:	**Auto**
Options: Disabled Auto	
ASPM Latency Checking:	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > SCH Control Sub-Menu > **SCH USB Control Sub-Menu**	
USB Client - Device 26, Function 0:	**Disabled**
Options: Disabled Enabled	
USB - Device 29, All Functions:	**Enabled**
Options: Disabled Enabled	
USB - Device 29, F2 Only:	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **Video (Intel IGD) Control Sub-Menu**	
IGD - Boot Type:	**CRT**
Options: VBIOS Default CRT LFP	
> IGD - LCD Control Sub-Menu	
Pre-Allocated Memory Size:	**8 MB**
Options: Disable 1 MB 4 MB 8 MB	
Graphic Memory Aperture Size:	**256 MB**
Options: 128 MB 256 MB	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Video (Intel IGD) Control Sub-Menu > **IGD - LCD Control Sub-Menu**	
IGD - LCD Panel Type:	**1024x768 generic**
Options: 640x480 generic 800x600 generic 1024x768 generic 640x480 NEC 8.4” 800x480 NEC 9” 1024x600 TMD 5.61” 1024x600 Samsung 4.8” 1024x768 Samsung 15” 1024x768 Sharp 7.2” 1280x800 Samsung 15.4” 11: Reserved 12: Reserved 13: Reserved 14: Reserved 15: Reserved 16: Reserved	
IGD - Panel Scaling:	**Auto**
Options: Auto Force Scaling Off	
GMCH BLC Control:	**GMBus**
Options: PWM GMBus	
BIA Control	**Disabled**
Options: Automatic Disabled Level 1 Level 2 Level 3 Level 4 Level 5 Level 6	
Spread Spectrum Clock Chip:	**Off**
Options: Off On	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Super I/O Control Sub-Menu

Serial port 1:		**Enabled**		
Speed:		**Low**		
Base I/O address:		**3F8**		
Interrupt:		**IRQ 4**		
Interface:		**RS232**		
Options:				
Port x: Disabled Enabled	**Speed:** Low High	**Base I/O address:** 3F8 2F8 3E8 2E8	**Interrupt:** Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7 IRQ 9 IRQ10 IRQ12	**Interface:** RS232 RS422 RTS RS422 Auto RS485 RTS RS485 RTS w/Echo RS485 Auto RS485 Auto w/Echo
Serial port 2:		**Enabled**		
Speed:		**Low**		
Base I/O address:		**2F8**		
Interrupt:		**IRQ 3**		
Interface:		**RS232**		
Options:				
Port x: Disabled Enabled	**Speed:** Low High	**Base I/O address:** 3F8 2F8 3E8 2E8	**Interrupt:** Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7 IRQ 9 IRQ10 IRQ12	**Interface:** RS232 RS422 RTS RS422 Auto RS485 RTS RS485 RTS w/Echo RS485 Auto RS485 Auto w/Echo
Serial port 3:		**Enabled**		
Speed:		**Low**		
Base I/O address:		**3E8**		
Interrupt:		**IRQ 5**		
Interface:		**RS232**		
Options:				
Port x: Disabled Enabled	**Speed:** Low High	**Base I/O address:** 3F8 2F8 3E8 2E8	**Interrupt:** Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7 IRQ 9 IRQ10 IRQ12	**Interface:** RS232 RS422 RTS RS422 Auto RS485 RTS RS485 RTS w/Echo RS485 Auto RS485 Auto w/Echo

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Super I/O Control Sub-Menu (continued)

Serial port 4:	**Enabled**
Speed:	**Low**
Base I/O address:	**2E8**
Interrupt:	**IRQ 6**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
			IRQ 9	RS485 Auto w/Echo
			IRQ10	
			IRQ12	

Parallel port:	**Enabled**
Base I/O address:	**378**
Interrupt:	**IRQ 7**

Options:

Port x:	**Base I/O address:**	**Interrupt:**
Disabled	378	Disabled
Enabled	278	IRQ 3
	3BC	IRQ 4
		IRQ 5
		IRQ 6
		IRQ 7
		IRQ 9
		IRQ 10
		IRQ12

Digital I/O port:	**Enabled**
DIO port address:	**120**
DIO IRQ:	**IRQ 10**

Options:

Digital I/O Port:	**DIO Port address:**	**DIO IRQ:**
Disabled	120	Disabled
Enabled	130	IRQ 3
	140	IRQ 4
		IRQ 5
		IRQ 6
		IRQ 7
		IRQ 9
		IRQ 10
		IRQ12

Watchdog:	**0**

Options:
{Enter any value between 0-255 for seconds.}

SIO Firmware:	Rev 0001

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ACPI Control Sub-Menu**	
Passive Cooling Trip Point:	**79 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive TC1 Value:	**1**
Passive TC2 Value:	**5**
Options: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
Passive TSP Value:	**10**
Options: 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150	
More CPU Thermal Control Sub-Menu options are continued on the next page.	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ACPI Control Sub-Menu** (continued)	
Critical Trip Point:	**POR**
Options: POR 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
FACP - RTC S4 Flag Value:	**Enabled**
Options: Disabled Enabled	
FACP - PM Timer Flag Value:	**Enabled**
Options: Disabled Enabled	
HPET Support:	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Security	
Supervisor Password Is:	Clear
User Password Is:	Clear
Set Supervisor Password:	**Enter**
Set User Password:	**Enter**
Fixed disk boot sector:	**Normal**
Options: Normal Write Protect	
Virus check reminder:	**Disabled**
Options: Disabled Daily Weekly Monthly	
System backup reminder:	**Disabled**
Options: Disabled Daily Weekly Monthly	
Password on boot:	Disabled
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Boot

Boot priority order:

1: **USB FDC**
2: **IDE0**
3: **IDE1**
4: **USB HDD**
5: **USB CDROM**
6: **PCI BEV**
7:
8:

Options:
IDE0
IDE1
USB FDC
USB HDD
USB CDROM
PCI BEV

Excluded from boot order:

Options:
USB ZIP
USB LS120
Other USB

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Exit
Exit Saving Changes
Exit Saving Changes to CMOS and EEPROM
Exit Discarding Changes
Load Setup Defaults
Discard Changes
Save Changes

BIOS SETTINGS STORAGE OPTIONS

CMOS Storage Locations

The EBC-Z5xx's BIOS configuration is stored in three (3) locations:

(1) CMOS RAM (nonvolatile if battery backed)

(2) EEPROM (nonvolatile storage for user defaults)

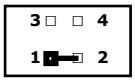
(3) FLASH PROM (nonvolatile storage for factory defaults)

Saving the CMOS Configuration

The Real-Time Clock and the CMOS RAM settings can be maintained by an optional battery when the board is powered off. The battery can be enabled/disabled with a jumper at **J43**. A battery is always required to maintain time and date functions when the board is powered off.

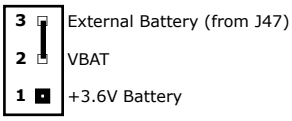
The EEPROM feature allows the user to save CMOS configuration settings to nonvolatile storage that does not require a battery. This feature can be enabled/disabled using **J33**. When enabled, the user's CMOS settings can be saved to EEPROM from the BIOS utility's Main Menu. If the board is powered off with no battery, the user's CMOS settings will be restored from EEPROM but time and date information will be lost and returned to default values.

J33



EEPROM Enable	
Enables EEPROM BIOS Settings (default)	1-2
Disables EEPROM BIOS Settings	3-4

J43



Enables On-board Battery	1-2
Enables External Battery (default)	2-3

At system boot, the BIOS first performs a checksum validation on the contents of the CMOS RAM. Invalid checksums usually occur due to a low or disabled battery. If the checksum is valid, the system boots using values stored in CMOS RAM. If a checksum error occurs, the BIOS attempts to load CMOS values from the EEPROM.

After a checksum validation, the BIOS configuration is loaded from the EEPROM and the boot process continues. If the EEPROM is disabled or the contents of the EEPROM fail the checksum validation, the system loads the factory default settings from the FLASH PROM and continues the boot sequence.

For applications where the battery is present, CMOS settings should be saved to both the CMOS RAM and to the EEPROM so the system can continue to function without user interaction.

Resetting CMOS to EEPROM defaults

If a battery is present, you can reset the CMOS RAM to the values stored in EEPROM by turning the system off and removing the jumper from **J43**. Replace the jumper and reboot. When power is applied to the board, the system will boot with the CMOS settings that were stored in EEPROM.

Resetting CMOS to EEPROM to Factory Defaults

The EBC-Z5xx can normally be returned to the factory default BIOS configuration by selecting option Load Setup Defaults on the BIOS Exit menu.

If you have saved EEPROM values that prevent you from accessing BIOS menus, the board can be reset to factory defaults as follows:

1) Turn the system off.
2) Move the jumper from pins 1-2 to 3-4 on **J33**.
3) Turn the system on and enter the BIOS Main Menu using the **F2** key.
4) Select Load Defaults from the Exit menu.
5) Move the jumper on pins 3-4 to 1-2 at **J33**.
6) Save the restored defaults to CMOS and EEPROM.

Updating the BIOS FLASH PROM

The most recent EBC-Z5xx BIOS is available on the WinSystems website. However, it is highly recommended that an Applications Engineer be consulted prior to any BIOS FLASH PROM update. If the BIOS PROM is updated, the steps described above must be followed to reset the CMOS and EEPROM to the newly loaded factory defaults and to clear the data from the previous BIOS version.

CABLES

Part Number	Description
CBL-SET-364-G-1	Cable set for EBC-Z5xx includes:
ADP-IO-USB-001	Dual 8-pin, 2-mm. 4 USB ports
CBL-173-G-1-1.0	20-pin ribbon to two 9-pin male D connector adapter
CBL-234-G-1-1.375	14-pin ribbon to 15-pin D-sub Analog VGA adapter
CBL-236-G-2-1.5	Power cable (unterminated)
CBL-247-G-1-1.0	1-ft., Multi-I/O adapter
CBL-270-G-2-1.5	5.1 Audio Access Cable
CBL-343-G-1-1.375	PS/2 Mouse Adapter
CBL-361-G-1-0.875	USB Dual (2 each)
BAT-LTC-E-36-16-1	External 3.6V, 1600 mAH battery with plug-in connector
Additional Cables	
CBL-115-4	4-ft., Opto rack interface
CBL-126-G-10-2.0	ATA100 IDE Disk Cable
CBL-355-G-1-1.5	HD Audio Extension
CBL-356-G-1-1.0	USB Dual
External Batteries	
BAT-LTC-E-36-27-1	External 3.6V, 2700 mAH battery with plug-in connector

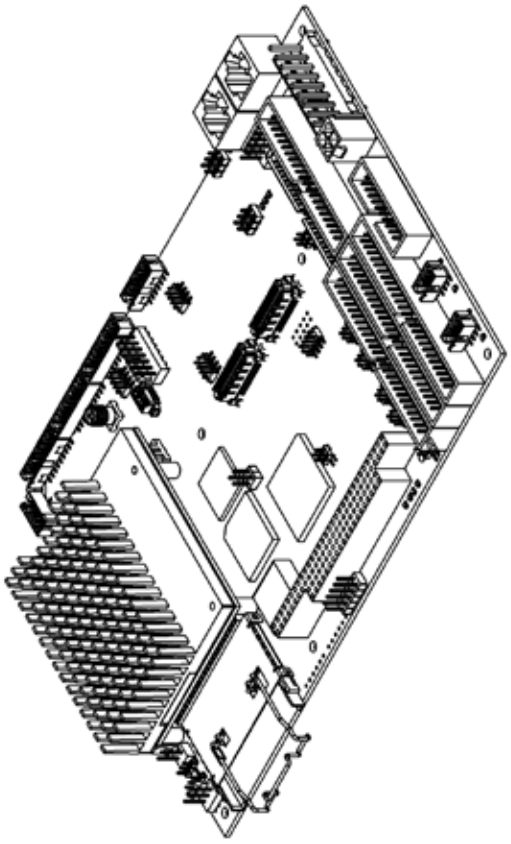
SOFTWARE DRIVERS

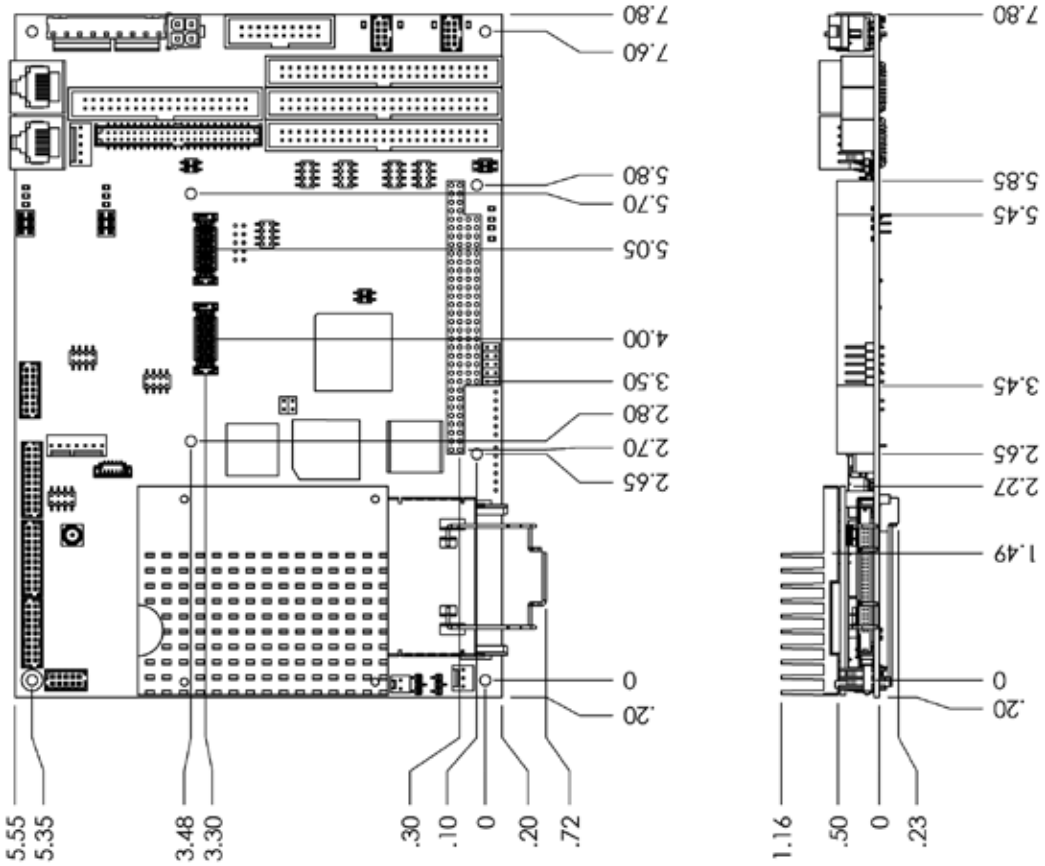
BIOS	
EBC-Z5xx BIOS	See WinSystems website.
Video Driver	
Windows XP	WinXP.zip
Audio Driver	
Windows XP (Intel)	Intel.zip
Windows XP (VIA)	v650a.zip
Gigabit Ethernet Driver	
Windows XP	Pro2KXP_v14_0.zip
WS16C48 Digital I/O Driver	
Windows XP	wsuio48_96xp.zip
Watchdog Timer Driver	
Windows XP	WSWDTXP.zip

SPECIFICATIONS

Electrical				
VCC	±5V ±5% required			
	EBC-Z510-G-512M-1 (1.1 GHz)		**EBC-Z530-G-512M-1 (1.6 GHz)**	
	Peak	1.9A	Peak	2.2A
	Typical	1.2A	Typical	1.25A
	Suspend	0.125A	Suspend	0.14A
Mechanical				
Dimensions	5.75” x 8.0” (147 mm x 203 mm)			
Weight	12.8 oz (363 g)			
Environmental				
Operating Temperature	-40°C to 60°C (1.6 GHz ATOM™ SBC)			
	-40°C to 70°C (1.1 GHz ATOM™ SBC)			

MECHANICAL DRAWING





APPENDIX - A

BEST PRACTICES

POWER SUPPLY

The power supply and how it is connected to the Single Board Computer (SBC) is very important.

Avoid Electrostatic Discharge (ESD)
Only handle the SBC and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget
Evaluate your power supply budget. It is usually good practice to budget 2X the typical power requirement for all of your devices.

Zero-Load Power Supply
Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply will not regulate properly and can cause damage to the SBC.

Use Proper Power Connections (Voltage)
When verifying the voltage, you should always measure it at the power connector on the SBC. Measuring at the power supply does not account for voltage drop through the wire and connectors.

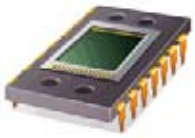
The single board computer requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers will have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the single board computer the better.

Adjusting Voltage
If you have a power supply that will allow you to adjust the voltage, it is a good idea to set the voltage at the power connector of the SBC to 5.1V. The SBC can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for a small amount of voltage drop that will occur over time as the power supply ages and the connector contacts oxidize.

Power Harness
Minimize the length of the power harness. This will reduce the amount of voltage drop between the power supply and the single board computer.

Gauge Wire
Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper will help your system perform properly over time.



Contact Points
WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion resulting in unreliable connections.

Pin Contacts
Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcons' design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

POWER DOWN

Make sure the system is **completely off/powered down** before connecting anything.

Power Supply OFF
The power supply should always be off before it is connected to the single board computer.

I/O Connections OFF
I/O Connections should also be off before connecting them to the single board computer or any I/O cards. Connecting hot signals can cause damage whether the single board computer is powered or not.

MOUNTING AND PROTECTING THE SINGLE BOARD COMPUTER

Do Not Bend or Flex the SBC
Never bend or flex the single board computer. Bending or flexing can cause irreparable damage. Single board computers are especially sensitive to flexing or bending around Ball-Grid-Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the single board computer can cause the BGA to tear away from the printed circuit board.

Mounting Holes
The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the single board computer's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

Never use a drill or any other tool in an attempt to make the holes larger.

Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.

Never use self-tapping screws; they will compromise the walls of the mounting hole.

Never use oversized screws that cut into the walls of the mounting holes.

Always use all of the mounting holes. By using all of the mounting holes you will provide the support the single board computer needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards
Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the single board computer to be flexed.

Avoid cutting of the SBC
Never use star washers or any fastening hardware that will cut into the single board computer.

Avoid Overtightening of Mounting Hardware
Causing the area around the mounting holes to compress could damage interlayer traces around the mouting holes.

Use Appropriate Tools
Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Placing the SBC on Mounting Standoffs
Be careful when placing the single board computer on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the single board computer.

Avoid Conductive Surfaces
Never allow the single board computer to be placed on a conductive surface. Almost all single board computers use a battery to backup the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

ADDING PC/104 BOARDS TO YOUR STACK

Be careful when adding PC/104 boards to your stack.

Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it will cause the I/O board to be damaged beyond repair.

OPERATIONS / PRODUCT MANUALS

Every single board computer has an Operations manual or Product manual.

Manual Updates
Operations/Product manuals are updated often. Periodicially check the WinSystems website (http://www.winsystems.com) for revisions.

Check Pinouts
Always check the pinout and connector locations in the manual before plugging in a cable. Many single board computers will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer with questions
If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact your Applications Engineer.

APPENDIX - B

POST CODES

If the system hangs before the BIOS can process the error, the value displayed at the I/O port I/O address 80h is the last test that performed. In this case, the screen does not display an error code.

The following is a list of the checkpoint codes written at the start of each test and their corresponding audio beep codes issued for terminal errors.

Code	Beeps	Location	Description
01h			IPMI initialization
02h			Verify real mode
03h			Disable non-maskable interrupt (NMI)
04h			Get CPU type
06h			Hardware initialization
07h			Chipset BIOS deshadow
08h			Chipset initialization
09h			Set IN POST flag
0Ah			CPU initialization
0Bh			CPU cache on
0Ch			Cache initialization
0Eh			I/O initialization
0Fh			FDISK initialization
10h			Power management initialization
11h			Register initialization
12h			Restore CR0
13h			PCI bus master reset
14h			8742 initialization (keyboard/embedded controller)
16h	1-2-2-3	Checksum BIOS ROM	
17h			Pre-size RAM (initialize cache before memory auto size)
18h			Timer initialization (8254 CTC)
1Ah			DMA initialization (8237 DMAC)
1Ch			Reset PIC (8259 PIC)
20h	1-3-1-1	Test DRAM refresh	
22h	1-3-1-3		Test 8742 Keyboard Controller
24h			Set huge ES (segment register to 4 GB)
26h			Enable A20
28h			Auto size DRAM
29h			POST memory manager (PMM) initialization
2Ah			Zero base (clear 512 KB base RAM)
2Bh			Enhanced CMOS initialization
2Ch	1-3-4-1	Address test (RAM failure on address line **xxxx***)	
2Eh	1-3-4-3	Base RAM Low (RAM failure on data bits **xxxx*** of low byte)	
2Fh			Pre-sys shadow (Enable cache before system BIOS shadow)
30h			Base RAM High (RAM failure on data bits **xxxx*** of high byte)
32h			Compute speed (test CPU bus-clock frequency)
33h			Post Dispatch Manager (PDM) initialization
34h			CMOS test
35h			Register re-initialization
36h			Check shutdown (perform warm restart)

Code	Beeps	Location	Description
37h			Chipset re-initialization
38h			System shadow (shadow BIOS ROM)
39h			Cache re-initialization
3Ah			Cache auto-size
3Bh			Debug server initialization
3Ch			Advanced chipset initialization
3Dh			Advanced register configuration
3Eh			Read hardware
3Fh			RomPilot memory initialization
40h			Speed
41h			RomPilot initialization
42h			Interrupt vectors initialization
44h			Set BIOS interrupt
45h			Device initialization
46h	2-1-2-3	Check ROM copyright	
48h			Config (Check video configuration against CMOS)
49h			PCI initialization
4Ah			Video initialization (Initialize all video adapters)
4Bh			QuietBoot start
4Ch			Video shadow (Shadow video BIOS)
4Eh			Copyright display
4Fh			MultiBoot-XP initialization
50h			CPU type display
51h			EISA initialization
52h			Keyboard test
54h			Set key click (if enabled)
55h			USB initialization
56h			Enabled keyboard
57h			1394 Firewire initialization
58h	2-2-3-1	HOT (Test for unexpected interrupts)	
59h			POST display service (PDS) initialization
5Ah			Display prompt **Press F2 to enter SETUP**
5Bh			CPU cache off
5Ch			Test RAM between 512 KB to 640 KB
60h			Test extended memory
62h			Test extended memory address
64h			Jumper to UserPatch1
66h			Configure advanced cache registers
67h			Initialize Multi Processor APIC
68h			Cache configuration (enable internal and external caches)
69h			PM setup System Management Mode (SMM)
6Ah			Display external L2 cache size
6Bh			Load custom defaults (optional)
6Ch			Display shadow-area messages
70h			Display error messages
72h			Check for configuration errors

Code	Beeps	Location	Description
74h			RTC test
76h			Keyboard test
7Ah			Key lock
7Ch			Hardware interrupts
7Dh			Intelligent System Monitoring (ISM) initialization
7Eh			Coprocessor initialization (if present)
80h			I/O initialization (before)
81h			Late device initialization
82h			RS-232 initialization
83h			FDISK config IDE
84h			LPT initialization
85h			PCI PCC initialization (PC-compatible PnP ISA devices)
86h			I/O initialization (after)
87h			Motherboard Configurable Devices (MCD) initialization
88h			BIOS data-area initialization (BDA)
89h			Enable Non-Maskable Interrupt (NMI)
8Ah			Extended BIOS Extended Data Area (EBDA)
8Bh			Mouse initialization
8Ch			Floppy initialization
8Fh			FDISK fast pre-initialization
90h			FDISK initialization
91h			FDISK fast initialization
92h			Jump to UserPatch2
93h			Build MPTABLE for multi-processor boards
95h			CDROM initialization
96h			Clear huge ES
97h			MultiProcessor table fix-up
98h	1-2		Option ROM scan
99h			FDISK check SMART
9Ah			Miscellaneous shadow (shadow option ROMs)
9Bh			PM CPU speed
9Ch			Power Management (PM) setup
9Dh			Intialize security engine
9Eh			IRQS
9Fh			FDISK fast initialization #2
A0h			Time of day - set
A2h			Keylock test
A4h			Key rate initialization (typematic rate)
A8h			Erase F2 prompt
AAh			Scan for F2 keystroke
ACh			Setup check
AEh			Clear bootflag
B0h			Error check
B1h			RomPilot unload
B2h			POST done - prepare to boot operating system
B4h	1		One beep (before boot)

Code	Beeps	Location	Description
B5h			Terminate QuietBoot
B6h			Check password
B7h			ACPI initialization
B8h			System initialization
B9h			Prepare to boot
BAh			DMI - SMBIOS initialization
BBh			BCV (Boot Connection Vectors) initialization
BCh			Parity - clear parity checkers
BDh			MultiBoot-XP boot menu display
BEh			Clear screen
BFh			Check reminders (virus and backup)
C0h			INT19 - boot
C1h			POST Error Manager (PEM) - Initialization
C2h			POST Error Manager (PEM) - Logging initialization
C3h			POST Error Manager (PEM) - Initialize error display function
C4h			POST Error Manager (PEM) - Initialize system error handler
C5h			PNP'ed dual CMOS
C6h			Initialize note dock
C7h			Initialize note dock late
C8h			Force check
C9h			Extended checksum

Embedded Extensions	
Code	**Description**
CAh	TP_SERIAL_KEY - Redirect INT15h to serial keyboard
CBh	TP_ROMRAM - Redirect INT13h to Memory Technologies Devices Such as ROM, RAM, PCMCIA, and serial disk
CCh	TP_SERIAL_VID - Redirect INT10h to enable remote serial video
CDh	TP_PCMATA - Re-map I/O and memory for PCMCIA
CEh	TP_PEN_INIT - Initialize digitizer and display message
CFh	TP_XBDA_FAIL - Extended BIOS Data Area (XBDA) failure

More Post Codes	
Code	**Description**
D1h	TP_BIOS_STACK_INIT
D3h	TP_SETUP_WAD
D4h	TP_CPU_GET_STRING
D5h	TP_SWITCH_POST_TABLES
D6h	TP_PCCARD_INIT
D7h	TP_FIRSTWARE_CHECK
D8h	TP_ASF_INIT
D9H	TP_IPMI_INIT_LATE
DAh	TP_PCIE_INIT
DBh	TP_SROM_TEST
DCh	TP_UPD_ERROR
DDh	TP_REMOTE_FLASH
DEh	TP_UNDI_INIT
DFh	TP_UNDI_SHUTDOWN
E0h	TP_EFI_NV_INIT
E1h	TP_PERIODIC_TIMER

Boot Block	
Code	**Description**
80h	TP_BB_CS_INIT - Chipset Init
81h	TP_BB_BRIDGE_INIT - Bridge Init
82h	TP_BB_CPU_UNIT - CPU Init
83h	TP_BB_TIMER_INIT - System timer Init
84h	TP_BB_IO_INIT - System I/O Init
85h	TP_BB_FORCE - Check force recovery boot
86h	TP_BB_CHKSUM - Check BIOS Checksum
87H	TP_BB_GOTOBIOS - Go to BIOS
88h	TP_BB_MP_INIT - Init Multi Processor
89h	TP_BB_SET_HUGE - Set Huge Seg
8Ah	TP_BB_OEM_INIT - OEM Special Init
8Bh	TP_BB_HW_INIT - Init PIC and DMA
8Ch	TP_BB_MEM_TYPE - Init Memory Type
8Dh	TP_BB_MEM_SIZE - Init Memory Size
8Eh	TP_BB_SHADOW - Shadow Boot Block
8Fh	TP_BB_SMM_INIT - Init SMM
90h	TP_BB_RAMTEST - System Memory Test
91h	TP_BB_VECS_INIT - Init Interrupt Vectors
92h	TP_BB_RTC_INIT - Init RTC
93h	TP_BB_VIDEO_INIT - Init Video
94h	TP_BB_OUT_INIT - Init Beeper
95h	TP_BB_BOOT_INIT - Init Boot
96h	TP_BB_CLEAR_HUGE - Clear Huge Seg
97h	TP_BB_BOOT_OS - Boot to OS
98h	TP_BB_USB_INIT - Intialize the USB Controller
99h	TP_BB_SECUR_INIT - Init Security

***** If the BIOS detects error 2C, 2E, or 30 (base 512 KB RAM error), it displays an additional word-bitmap (**xxxx**) indicating the address line or bits that failed.

For example, “2C 0002” means address line 1 (bit one set) has failed. “2E 1020” means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80h LED display. It first displays the checkpoint code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

WARRANTY INFORMATION

(http://www.winsystems.com/company/warranty.cfm)

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2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.