



COMIT

Computer On Module Interconnect Technology™

SPECIFICATION

Revision 1.1

September 22, 2009

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Revision History

Revision	Issue Date	Comments
1.0	March 2, 2009	Initial Release
1.1	Sept 22, 2009	Update pin definition for power architecture

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1.0 Introduction

1.1 General

COMIT is an electromechanical connectorization specification for Computer On Module (COM) processor products that integrate common high-speed and low-speed serial as well as legacy expansion buses for next generation, small form factor products. It is a modular, high-speed connector system composed of the most common high speed and legacy interfaces available from modern low-power chipsets. The purpose is to provide a compact, interoperable processor connection architecture for future embedded systems designs.

COMIT supports different processors with a single baseboard, allowing easy migration to future processors for performance/feature enhancement, and mitigating obsolescence for either the processor or baseboard. COMIT is processor independent, focusing on bus and interconnect technology rather than any single processor, DSP, or microcontroller architecture.

The COMIT acronym stands for Computer On Module Interconnect Technology and is pronounced “Com it”.

In a single connector, COMIT supports:

- Three x1 (pronounced “by one”) PCI Express™ links
- One x4 (“by four”) PCI Express link (optionally 4 divided into 4 additional x1 links)
- Six high-speed USB 2.0 channels
- VGA, digital video, and dual 18/24 bit LVDS video interfaces
- Two SATA channels
- One 10/100 or Gigabit Ethernet
- One 8 bit SDIO
- HD Audio
- LPC (Low Pin Count) Bus
- SPI/uWire, SMBus/I²C Bus
- Power and ground
- System clock and control signaling

1.2 Audience

This document is written for design engineers, technologists, and others that desire to understand the basics of COMIT. It does not specify the connector mounting location or application of the technology to any specific computer module or I/O board. That information will be provided and explained in the specification that governs the implementation of COMIT technology on the particular form-factor.

Since COMIT supports multiple high-speed differential serial buses, care must be exercised with respect to best layout practice for high-speed signals. Please reference the websites listed in the next section for their design recommendations. Also visit the SFF-SIG website for any application notes or design guides that may be available.

1.3 Related Documents and Organizations

I²C Specification

NXP Semiconductors Netherlands B.V. (formerly Philips Semiconductors)
Eindhoven, Netherlands
http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

Low Pin Count (LPC) Specification

Intel Corporation
Santa Clara, CA USA
<http://www.intel.com/design/chipsets/industry/lpc.htm>

MiniBlade Specification

Small Form Factor Special Interest Group
2784 Homestead Road #269
Santa Clara, CA 95051 USA
Phone: +1-650-961-2473
www.sff-sig.org

PCI Express Specification

PCI-SIG
3855 SW 153rd Drive
Beaverton, OR 97006 USA
Phone: +1-503-619-0569 Fax: +1-503-644-6708
www.pcisig.com

Samtec, Inc. (Connector data)

520 Park East Boulevard
New Albany, IN 47151-1147 USA
Phone: +1-812-944-6733 Fax: +1-812-948-5047
www.samtec.com

SFF-SIG

Small Form Factor Special Interest Group
2784 Homestead Road #269
Santa Clara, CA 95051 USA
Phone: +1-650-961-2473
www.sff-sig.org

SMBus Specification

System Management Interface Forum, Inc.
100 N. Central Expressway Suite 600
Richardson, Texas 75080-5323 USA
Fax: +1-972-238-1286
www.smbus.org

SPI

The SPI bus is a *de facto* standard, rather than one agreed by any international committee. The reason for this is its essential simplicity. The best reference is http://www.freescale.com/files/microcontrollers/doc/ref_manual/S12SPIV3.pdf

USB

USB Implementers Forum, Inc.
3855 SW 153rd Drive
Beaverton, OR 97006
www.usb.org

2.0 Acronyms and Terms

ATX-style	Refers to the power supply configuration that allows the computer to be turned off via software. ATX power supplies have two separate five volt signals, one that powers up and down with the system (+5V) and one that stays powered all of the time unless the supply is disconnected from the system power (+5VSB, standby) in order for the system to be capable of waking up from network traffic, keyboard, etc.
FWH	Abbreviation for Firmware Hub.
I ² C	The Inter-Integrated Circuit bus (I ² C) is a patented interface developed by Philips Semiconductors. The I ² C bus is a half-duplex, synchronous, multi-master bus requiring only two signal wires: data and clock.
Lane	A PCI Express link is built around dedicated unidirectional couples of serial (1-bit), point-to-point connections known as "lanes". PCI Express lanes are full-duplex links, meaning that data can be transferred in both directions simultaneously (Tx transmit and Rx receive lines are separate).
Link	A connection between any two PCI Express devices is known as a "link", and is built up from a collection of one or more lanes. All devices must minimally support single-lane (x1) link.
LPC Bus	<p>Low Pin Count Bus -- It is used on embedded PCs to connect low-bandwidth devices to the CPU, such as the boot ROM and the "legacy" I/O devices. The "legacy" I/O devices usually include serial ports, parallel ports, keyboard, mouse, and floppy disk controller. Designers will benefit from the reduced pin count because it uses less space and power, and is more thermally efficient compared to ISA.</p> <p>The LPC specification defines seven mandatory signals required for bidirectional data transfer. Four of these signals carry the multiplexed address and data. The other three are control signals (frame, reset, and clock).</p>
LVDS	Abbreviation for Low Voltage Differential Signaling which is used to connect to flat panel displays.

MiniBlade™	A removable Flash storage solution for embedded SBCs administered by the SFF-SIG.
PCI Express	It is a high-speed computer expansion card interface designed to replace the general-purpose PCI expansion bus and is software compatible with PCI in order to be transparent to system software. It is structured around point-to-point full duplex serial links called lanes. In PCI Express version 1.1 (currently the most common version), each lane operates at a data rate of 250 MB/s in each direction. COMIT supports three single lanes and one quad lane of data between the baseboard and expansion card. Lane counts are written with an “x” prefix with “x1” designating a single-lane and “x4” for a four-lane interface. A x1 (pronounced “by one”) lane is very space efficient compared to the parallel PCI bus that it replaces, with 2.5 times the bandwidth using only five signals. Four lanes of 250 MB/s in a x4 link supports a maximum transfer rate of 1 GB/s (250 MB/s x4) in each direction for PCIe 1.1.
PCIe	Abbreviation for PCI Express.
SATA	The Serial ATA computer bus is a high-speed serial interface for connecting controllers to mass storage devices such as hard disks
SBC	Abbreviation for Single Board Computer.
SDVO	Serial Digital Video Out is a technology that allows additional video signaling interfaces such as VGA and DVI monitor outputs, SDTV and HDTV television outputs, or TV tuner inputs to a system board
SFF-SIG	The Small Form Factor Special Interest Group is an independent non-profit industry group that develops, promotes, and supports small form factor circuit board, I/O, and storage specifications with long-term stability in mind.
SEARAY™	The name of a 0.50” [1.27mm] pitch high density, high-speed board-to-board interconnect system.
SMBus	System Management Bus – A simple two-wire bus, derived from I ² C and used in the x86 architecture for communication with low-bandwidth devices such as memory sticks, clock generators, and temperature sensors.
SPI	Serial Peripheral Interface Bus — A synchronous serial data link standard named by Motorola that operates in full duplex mode.
SUMIT™	Abbreviation for <u>S</u> tackable <u>U</u> nified <u>M</u> odule <u>I</u> nterconnect <u>T</u> echnology specification administered by the SFF-SIG.

USB	Universal Serial Bus — It is a serial bus designed to allow peripherals to be connected using a single standardized interface which replaces certain legacy varieties of serial and parallel ports.
uWire	Microwire is a three-wire synchronous interface developed by National Semiconductor. The Microwire protocol is essentially a subset of the SPI interface. Microwire/Plus with alternate shift clock is compatible with SPI mode 0. Microwire with standard shift clock is compatible with SPI mode 1.

3.0 COMIT Connector

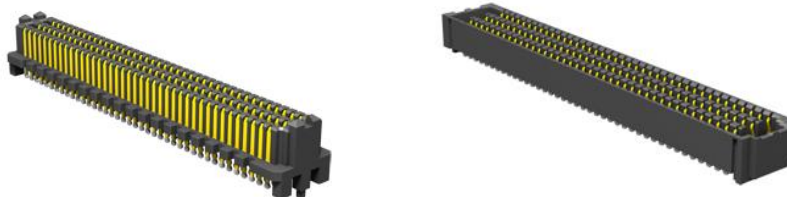
3.1 SEARAY Series High Speed Board-to-Board Interconnect

Computer On Module connector requirements for modern chipsets used in rugged environments represent a significant challenge for the connector vendor. For PCI Express 2.0 and USB3 signaling requirements, connectors should be selected with bandwidth well in excess of the 5GT/S requirements of both. Connectors must also be very dense for these applications as both the module and chip scales shrink. Connectors that combine the best speed and density often fall short as far as reliability in rugged applications, or are very expensive.

The SEARAY connector from Samtec embodies all of the requirements- high speed, high pin density, rugged and low cost. It is a 240-pin high-density (0.050-inch pitch) SEAM/SEAF connector pair. The connector series is second sourced by Molex. SEARAY is designed as an open pin field array configuration organized as six rows of 40 gold-plated pins to allow optimal routing and maximum design flexibility. The chosen connector system is capable of a differential signaling rate of 9 GHz bandwidth (at -3dB insertion loss) to support current and future high speed signaling for interfaces like PCI Express Gen2 and USB3.

SEAM: ASP-140867-01

SEAF: ASP-140868-01



SEARAY Connectors from Samtec

The contacts in the SEARAY system are robust and allow for “zippering” when mating and unmating the connectors. This contact design lowers the insertion and extraction forces which is an important consideration with 240 pins. Each pin is rated for 2.7 Amps and the connector will operate over the temperature range of -55°C to +125°C. The

rugged connector system is good for over 2000 mating cycles, is RoHS compliant, and is ideal for industrial environments.

The SEARAY connector series are specified for use with or without standoffs. The mated height of the connector pair is 8.5mm without standoffs, 8.65mm with standoffs. The SEAF standard part number is ASP-140868-01 (Std. Part: SEAF-40-05.0-S-06-2-A, processor board) and the SEAM standard part number is ASP-140867-01 (Std. Part: SEAM-40-03.5-S-06-2-A, baseboard). Detailed data sheets can be found at <http://www.samtec.com/search/comit.aspx>.

3.1.1 Connector Stack Height

The stack height is measured from the top of the baseboard to the bottom of the processor module (assuming the processor is on top). An 8.5mm mated connector height has been chosen to allow for component height between processor and baseboard while minimizing overall height.

For non-rugged applications, the SEAF/SEAM connector pair is specified to be used without standoffs at an 8.5mm nominal height. For rugged configurations, the 8.5mm version of the SEAF/SEAM connector pair is engineered to optimize manufacturing tolerances of standoff hardware and their buildup in COM and mezzanine module implementations using the same connectors. Samtec manufactures a standoff specifically for the 8.5mm SEAF/SEAM pair that is 8.65mm overall with male 4-40 threads on one end, female on the other. The use of this 8.65mm standoff height is specifically tailored to the mechanical requirements of the SEAF/SEAM pair and produces an extremely rugged connector solution. The 8.65mm standoff part number from Samtec is ASP-144136-01.

Component maximum height is specified to be 5.4mm for the processor module (on the COMIT connector side) and 3.0mm maximum height for the baseboard (again on the COMIT connector side). These specifications apply for the entire area between the two boards to prevent mechanical interference issues when modules are plugged into baseboards.

3.1.2 Connector Placement

The SEAF is the connector on the COMIT processor module and the SEAM is the baseboard connector. This specification does not address the location (placement) requirements for any specific form factor. Please refer to the separate form factor specifications for detailed COMIT connector placement information.

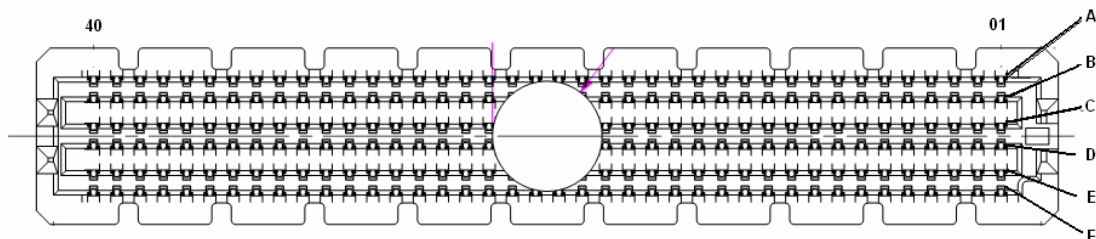
3.2 Connector Pin Assignments

COMIT was designed to support x86 architectures as well as any other processor or DSP requiring the unique mix of interfaces available on the COMIT connector. As long as the design guidelines for interfacing are followed, DSPs, micros, MIPS, RISC, and

other non-x86 processor architectures are all compatible. This enables the unique ability to connect either an x86, DSP, or Xscale processor module to the same baseboard for a diverse product offering if desired.

COMIT connector pin assignments are optimized for signal integrity, relative layout ease, and optimal routing with small form factor chipset and processor solutions available from Intel and VIA Technologies. Implementation of other chipsets and architectures are supported as well.

COMIT is engineered to be completely complimentary to the SUMIT, MiniBlade, and other architectures developed and published by the SFF-SIG.



COMIT Baseboard SEAM Connector Pin Locations

3.2.1 I/O Connector Row A and Row B Pin Assignments

Pin A1	C_PERn0
Pin A2	C_PERp0
Pin A3	GND
Pin A4	C_PETn0
Pin A5	C_PETp0
Pin A6	CPRSNT#/GND
Pin A7	C_CLKn
Pin A8	C_CLKp
Pin A9	GND
Pin A10	A_PERn0
Pin A11	A_PERp0
Pin A12	GND
Pin A13	A_PETn0
Pin A14	A_PETp0
Pin A15	APRSNT#/GND
Pin A16	A_CLKn
Pin A17	A_CLKp
Pin A18	GND
Pin A19	B_PERn0
Pin A20	B_PERp0
Pin A21	GND
Pin A22	B_PETn0
Pin A23	B_PETp0
Pin A24	BPRSNT#/GND
Pin A25	B_CLKn
Pin A26	B_CLKp
Pin A27	GND
Pin A28	D_PETn3
Pin A29	D_PETp3
Pin A30	GND
Pin A31	D_PETn2
Pin A32	D_PETp2
Pin A33	GND
Pin A34	D_PERn3
Pin A35	D_PERp3
Pin A36	GND
Pin A37	D_PERn1
Pin A38	D_PERp1
Pin A39	GND
Pin A40	PERST#

Pin B1	GND
Pin B2	USB4+
Pin B3	USB4-
Pin B4	GND
Pin B5	USB2+
Pin B6	USB2-
Pin B7	GND
Pin B8	USB0+
Pin B9	USB0-
Pin B10	GND
Pin B11	SDVO_R+
Pin B12	SDVO_R-
Pin B13	GND
Pin B14	SDVO_G+
Pin B15	SDVO_G-
Pin B16	GND
Pin B17	SDVO_INT+
Pin B18	SDVO_INT-
Pin B19	GND
Pin B20	SDVO_B+
Pin B21	SDVO_B-
Pin B22	GND
Pin B23	SDVO_CLK+
Pin B24	SDVO_CLK-
Pin B25	GND
Pin B26	SDVO_CNTDAT
Pin B27	SDVO_CNTLCLK
Pin B28	BL_ENA
Pin B29	LVDS_DDCDAT
Pin B30	LVDS_DDCCLK
Pin B31	GND
Pin B32	D_PETn1
Pin B33	D_PETp1
Pin B34	GND
Pin B35	D_PERn2
Pin B36	D_PERp2
Pin B37	GND
Pin B38	D_PERn0
Pin B39	D_PERp0
Pin B40	GND

3.2.2 I/O Connector Row C and Row D Pin Assignments

Pin C1	USB5+
Pin C2	USB5-
Pin C3	GND
Pin C4	USB3+
Pin C5	USB3-
Pin C6	GND
Pin C7	USB1+
Pin C8	USB1-
Pin C9	GND
Pin C10	SATA1_A+
Pin C11	SATA1_A-
Pin C12	GND
Pin C13	SATA1_B+
Pin C14	SATA1_B-
Pin C15	SATA1_SPINUP
Pin C16	GND
Pin C17	SATA0_SPINUP
Pin C18	SATA0_A+
Pin C19	SATA0_A-
Pin C20	GND
Pin C21	SATA0_B+
Pin C22	SATA0_B-
Pin C23	GND
Pin C24	ENET_X0+
Pin C25	ENET_X0-
Pin C26	GND
Pin C27	ENET_X1+
Pin C28	ENET_X1-
Pin C29	GND
Pin C30	ENET_X2+
Pin C31	ENET_X2-
Pin C32	GND
Pin C33	ENET_X3+
Pin C34	ENET_X3-
Pin C35	GND
Pin C36	D_CLKn
Pin C37	D_CLKp
Pin C38	DPRSNT#/GND
Pin C39	D_PETn0
Pin C40	D_PETp0

Pin D1	LPC_AD2
Pin D2	SERIRQ#
Pin D3	LPC_AD1
Pin D4	LPC_AD0
Pin D5	LPC_AD3
Pin D6	LPC_FRAME#
Pin D7	LPC_DRQ
Pin D8	CLK_33MHZ
Pin D9	LVDS_PWR_EN
Pin D10	GND
Pin D11	LVDS0_CLK+
Pin D12	LVDS0_CLK-
Pin D13	3.3V
Pin D14	LVDS0_Y3+
Pin D15	LVDS0_Y3-
Pin D16	3.3V
Pin D17	LVDS0_Y2+
Pin D18	LVDS0_Y2-
Pin D19	3.3V
Pin D20	LVDS0_Y1+
Pin D21	LVDS0_Y1-
Pin D22	3.3V
Pin D23	LVDS0_Y0+
Pin D24	LVDS0_Y0-
Pin D25	3.3V
Pin D26	LVDS1_CLK+
Pin D27	LVDS1_CLK-
Pin D28	+5V
Pin D29	LVDS1_Y3+
Pin D30	LVDS1_Y3-
Pin D31	+5V
Pin D32	LVDS1_Y2+
Pin D33	LVDS1_Y2-
Pin D34	+5V
Pin D35	LVDS1_Y1+
Pin D36	LVDS1_Y1-
Pin D37	+5V
Pin D38	LVDS1_Y0+
Pin D39	LVDS1_Y0-
Pin D40	GND

3.2.3 I/O Connector Row E and Row F Pin Assignments

Pin E1	CLK14	Pin F1	SDIO_D0
Pin E2	RSTBTN#	Pin F2	SDIO_D1
Pin E3	PWRBTN#	Pin F3	SDIO_D2
Pin E4	SLP_S3#	Pin F4	SDIO_D3
Pin E5	SLP_S4/S5#	Pin F5	SDIO_D4
Pin E6	ALLSYS_PWRGOOD	Pin F6	SDIO_D5
Pin E7	SMI	Pin F7	SDIO_D6
Pin E8	WAKE#	Pin F8	SDIO_D7
Pin E9	VBAT	Pin F9	SDIO_CMD
Pin E10	Reserved	Pin F10	SDIO_CLK
Pin E11	+3.3VSB	Pin F11	SDIO_WP
Pin E12	SPI/uWire_DO	Pin F12	SDIO_CD#
Pin E13	SPI/uWire_DI	Pin F13	SDIO_LED
Pin E14	SPI/uWire_CLK	Pin F14	SDIO_PWR
Pin E15	SPI/uWire_CS0#	Pin F15	Reserved
Pin E16	SPI/uWire_CS1#	Pin F16	Reserved
Pin E17	USB_OC#	Pin F17	HAD_RST#
Pin E18	USB_EN	Pin F18	HDA_SYNC
Pin E19	USB_CLIENTDET	Pin F19	HDA_SDO
Pin E20	RXD	Pin F20	HDA_SDI
Pin E21	TXD	Pin F21	HDA_CLK
Pin E22	LED0	Pin F22	HDA_SPKR
Pin E23	LED1	Pin F23	Reserved
Pin E24	GND	Pin F24	SMB/I2C_DATA
Pin E25	VGA_R	Pin F25	SMB/I2C_CLK
Pin E26	VGA_G	Pin F26	SMB/I2C_ALERT#
Pin E27	VGA_B	Pin F27	Reserved
Pin E28	VGA_HS	Pin F28	Reserved
Pin E29	VGA_VS	Pin F29	Reserved
Pin E30	VGA_DDCDAT	Pin F30	Reserved
Pin E31	VGA_DDCCLK	Pin F31	Reserved
Pin E32	Reserved	Pin F32	Reserved
Pin E33	+5VSB	Pin F33	Reserved
Pin E34	+5VSB	Pin F34	Reserved
Pin E35	+5V	Pin F35	Reserved
Pin E36	+5V	Pin F36	Reserved
Pin E37	+5V	Pin F37	Reserved
Pin E38	+5V	Pin F38	Reserved
Pin E39	+5V	Pin F39	Reserved
Pin E40	+5V	Pin F40	Reserved

3.3 COMIT Connector Signal Descriptions

PCI Express

Signal Name	Pin #	Description
A_PETp0	A14	PCIe link A, lane 0, Diff Pair transmit positive pin
A_PETn0	A13	PCIe link A, lane 0, Diff Pair transmit negative pin
A_PERp0	A11	PCIe link A, lane 0, Diff Pair receive positive pin
A_PERn0	A10	PCIe link A, lane 0, Diff Pair receive negative pin
A_CLKp	A17	PCIe link A, clock Diff Pair positive pin
A_CLKn	A16	PCIe link A, clock Diff Pair negative pin
APRSNT#/GND	A15	PCIe link A card present signal (driven by I/O card)
B_PETp0	A23	PCIe link B, lane 0, Diff Pair transmit positive pin
B_PETn0	A22	PCIe link B, lane 0, Diff Pair transmit negative pin
B_PERp0	A20	PCIe link B, lane 0, Diff Pair receive positive pin
B_PERn0	A19	PCIe link B, lane 0, Diff Pair receive negative pin
B_CLKp	A26	PCIe link B, clock Diff Pair positive pin
B_CLKn	A25	PCIe link B, clock Diff Pair negative pin
BPRSNT#/GND	A24	PCIe link C card present signal (driven by I/O card)
C_PETp0	A5	PCIe link C, lane 0, Diff Pair transmit positive pin
C_PETn0	A4	PCIe link C, lane 0, Diff Pair transmit negative pin
C_PERp0	A2	PCIe link C, lane 0, Diff Pair receive positive pin
C_PERn0	A1	PCIe link C, lane 0, Diff Pair receive negative pin
C_CLKp	A8	PCIe link C, clock Diff Pair positive pin
C_CLKn	A7	PCIe link C, clock Diff Pair negative pin
CPRSNT#/GND	A6	PCIe link C card present signal (driven by I/O card)
D_PETp0	C40	PCIe link D, lane 0, Diff Pair transmit positive pin
D_PETn0	C39	PCIe link D, lane 0, Diff Pair transmit negative pin
D_PERp0	B39	PCIe link D, lane 0, Diff Pair receive positive pin
D_PERn0	B38	PCIe link D, lane 0, Diff Pair receive negative pin
D_PETp1	B33	PCIe link D, lane 1, Diff Pair transmit positive pin
D_PETn1	B32	PCIe link D, lane 1, Diff Pair transmit negative pin
D_PERp1	A38	PCIe link D, lane 1, Diff Pair receive positive pin
D_PERn1	A37	PCIe link D, lane 1, Diff Pair receive negative pin
D_PETp2	A32	PCIe link D, lane 2, Diff Pair transmit positive pin
D_PETn2	A31	PCIe link D, lane 2, Diff Pair transmit negative pin
D_PERp2	B36	PCIe link D, lane 2, Diff Pair receive positive pin
D_PERn2	B35	PCIe link D, lane 2, Diff Pair receive negative pin
D_PETp3	A29	PCIe link D, lane 3, Diff Pair transmit positive pin
D_PETn3	A28	PCIe link D, lane 3, Diff Pair transmit negative pin
D_PERp3	A35	PCIe link D, lane 3, Diff Pair receive positive pin
D_PERn3	A34	PCIe link D, lane 3, Diff Pair receive negative pin
D_CLKp	C37	PCIe link D, clock Diff Pair positive pin
D_CLKn	C36	PCIe link D, clock Diff Pair negative pin
DPRSNT#/GND	C38	PCIe link D card present signal (driven by I/O card)
PERST#	A40	PCI Express reset signal

USB

Signal Name	Pin #	Description
USB0+	B8	USB Channel 0 Diff Pair positive
USB0-	B9	USB Channel 0 Diff Pair negative
USB1+	C7	USB Channel 1 Diff Pair positive
USB1-	C8	USB Channel 1 Diff Pair negative
USB2+	B5	USB Channel 2 Diff Pair positive
USB2-	B6	USB Channel 2 Diff Pair negative
USB3+	C4	USB Channel 3 Diff Pair positive
USB3-	C5	USB Channel 3 Diff Pair negative
USB4+	B2	USB Channel 4 Diff Pair positive
USB4-	B3	USB Channel 4 Diff Pair negative
USB5+	C1	USB Channel 5 Diff Pair positive
USB5-	C2	USB Channel 5 Diff Pair negative
USB_OC#	E17	USB Channels Overcurrent flag (wire OR)
USB_EN#	E18	USB Channels Enable Output (wire OR)
USB_CLIENTDET	E19	USB Channel Client Detect Input

SATA Port 0

Signal Name	Pin #	Description
SATA0_A+	C18	SATA Data Diff Pair A Positive
SATA0_A-	C19	SATA Data Diff Pair A Negative
SATA0_B+	C21	SATA Data Diff Pair B Positive
SATA0_B-	C22	SATA Data Diff Pair B Negative
SATA0_SPINUP	C17	SATA Spin Up Signal

SATA Port 1

Signal Name	Pin #	Description
SATA1_A+	C10	SATA Data Diff Pair A Positive
SATA1_A-	C11	SATA Data Diff Pair A Negative
SATA1_B+	C13	SATA Data Diff Pair B Positive
SATA1_B-	C14	SATA Data Diff Pair B Negative
SATA1_SPINUP	C15	SATA Spin Up Signal

VGA

Signal Name	Pin #	Description
VGA_R	E25	VGA Red
VGA_G	E26	VGA Green
VGA_B	E27	VGA Blue
VGA_HS	E28	VGA Horizontal Sync
VGA_VS	E29	VGA Vertical Sync
VGA_DDCDAT	E30	VGA PnP Data
VGA_DDCCLK	E31	VGA PnP Clock

LVDS Port 0

Signal Name	Pin #	Description
LVDS0_Y0+	D23	LVDS Data Diff Pair 0 Positive
LVDS0_Y0-	D24	LVDS Data Diff Pair 0 Negative
LVDS0_Y1+	D20	LVDS Data Diff Pair 1 Positive
LVDS0_Y1-	D21	LVDS Data Diff Pair 1 Negative
LVDS0_Y2+	D17	LVDS Data Diff Pair 2 Positive
LVDS0_Y2-	D18	LVDS Data Diff Pair 2 Negative
LVDS0_Y3+	D14	LVDS Data Diff Pair 3 Positive
LVDS0_Y3-	D15	LVDS Data Diff Pair 3 Negative
LVDS0_CLK+	D11	LVDS Clock Diff Pair 0 Positive
LVDS0_CLK-	D12	LVDS Clock Diff Pair 0 Negative

LVDS Port 1

Signal Name	Pin #	Description
LVDS1_Y0+	D38	LVDS Data Diff Pair 0 Positive
LVDS1_Y0-	D39	LVDS Data Diff Pair 0 Negative
LVDS1_Y1+	D35	LVDS Data Diff Pair 1 Positive
LVDS1_Y1-	D36	LVDS Data Diff Pair 1 Negative
LVDS1_Y2+	D32	LVDS Data Diff Pair 2 Positive
LVDS1_Y2-	D33	LVDS Data Diff Pair 2 Negative
LVDS1_Y3+	D29	LVDS Data Diff Pair 3 Positive
LVDS1_Y3-	D30	LVDS Data Diff Pair 3 Negative
LVDS1_CLK+	D26	LVDS Clock Diff Pair 0 Positive
LVDS1_CLK-	D27	LVDS Clock Diff Pair 0 Negative

LVDS Control

Signal Name	Pin #	Description
LVDS_DDCDAT	B29	LVDS PnP Data
LVDS_DDCCLK	B30	LVDS PnP Clock
BL_ENA	B28	LVDS Back Light Enable
LVDS_PWR_EN	D9	LVDS Panel Power Enable

Digital Video

Signal Name	Pin #	Description
SDVO_R+	B11	SDVO Red Diff Pair Positive
SDVO_R-	B12	SDVO Red Diff Pair Negative
SDVO_G+	B14	SDVO Green Diff Pair Positive
SDVO_G-	B15	SDVO Green Diff Pair Negative
SDVO_B+	B20	SDVO Blue Diff Pair Positive
SDVO_B-	B21	SDVO Blue Diff Pair Negative
SDVO_INT+	B17	SDVO Interrupt Diff Pair Positive
SDVO_INT-	B18	SDVO Interrupt Diff Pair Negative
SDVO_CLK+	B23	SDVO Clock Diff Pair Positive
SDVO_CLK-	B24	SDVO Clock Diff Pair Negative
SDVO_CNTDAT	B26	SDVO Control Data
SDVO_CNTCLK	B27	SDVO Control Clock

ETHERNET

Signal Name	Pin #	Description
ENET_X0+	C24	ENET Data Diff Pair 0 Positive
ENET_X0-	C25	ENET Data Diff Pair 0 Negative
ENET_X1+	C27	ENET Data Diff Pair 1 Positive
ENET_X1-	C28	ENET Data Diff Pair 1 Negative
ENET_X2+	C30	ENET Data Diff Pair 2 Positive
ENET_X2-	C31	ENET Data Diff Pair 2 Negative
ENET_X3+	C33	ENET Data Diff Pair 3 Positive
ENET_X3-	C34	ENET Data Diff Pair 3 Negative
LED0	E22	ENET Link/Activity LED
LED1	E23	ENET Speed LED

SDIO

Signal Name	Pin #	Description
SDIO_D0	F1	SDIO Data 0
SDIO_D1	F2	SDIO Data 1
SDIO_D2	F3	SDIO Data 2
SDIO_D3	F4	SDIO Data 3
SDIO_D4	F5	SDIO Data 4
SDIO_D5	F6	SDIO Data 5
SDIO_D6	F7	SDIO Data 6
SDIO_D7	F8	SDIO Data 7
SDIO_CMD	F9	SDIO Command
SDIO_CLK	F10	SDIO Clock
SDIO_WP	F11	SDIO Write Protect
SDIO_CD#	F12	SDIO Card Detect
SDIO_LED	F13	SDIO LED
SDIO_PWR	F14	SDIO Power enable Output

HD Audio

Signal Name	Pin #	Description
HDA_SDO	F19	HD Audio Serial Data Out
HDA_SDI	F20	HD Audio Serial Data In
HDA_CLK	F21	HD Audio Clock
HDA_RST#	F17	HD Audio Reset
HDA_SYNC	F18	HD Audio Sync
HDA_SPKR	F22	Speaker out to CODEC

SPI/uWire

Signal Name	Pin #	Description
SPI/uWire_DO	E12	Serial Data Out from Master, 3.3V
SPI/uWire_DI	E13	Serial Data In to Master, 3.3V
SPI/uWire_CLK	E14	Serial Clock
SPI/uWire_CS0#	E15	Chip Select for Device 0
SPI/uWire_CS1#	E16	Chip Select for Device 1

SMBus/I²C

Signal Name	Pin #	Description
SMB/I2C_DATA	F24	SMBus Data
SMB/I2C_CLK	F25	SMBus Clock
SMB/I2C_ALERT#	F26	SMBus Interrupt Line In

LPC

Signal Name	Pin #	Description
LPC_AD0	D4	LPC Address, Data, and Control Line 0
LPC_AD1	D3	LPC Address, Data, and Control Line 1
LPC_AD2	D1	LPC Address, Data, and Control Line 2
LPC_AD3	D5	LPC Address, Data, and Control Line 3
LPC_FRAME#	D6	LPC Frame Signal to Start or Terminate Cycles
SERIRQ#	D2	Serial IRQ for legacy interrupts
LPC_DRQ	D7	LPC DMA Request
CLK_33MHz	D8	33 MHz Clock Out

System Control

Signal Name	Pin #	Description
ALLSYS_PWRGOOD	E6	S0 Power Good Signal
SLP_S3#	E4	S3 Suspend to Ram Control
SLP_S4/S5#	E5	S4 Suspend to Disk / S5 Soft Off Control
PWRBTN#	E3	Momentary - Power On Input
SMI	E7	System Management Interrupt
CLK14	E1	14.31818 MHz Clock Output
RSTBTN#	E2	Momentary - Reset Button Input
WAKE#	E8	System Wake Signal

Serial

Signal Name	Pin #	Description
TXD	E21	Serial Data Out, 3.3V
RXD	E20	Serial Data in, 3.3V

Power and Ground

Signal Name	Pin #	Description
+5V	D28, D31, D34, D37, E35, E36, E37, E38, E39, E40	+5 volt power
+5VSB	E33, E34	Standby +5V (for ATX-style)
+3VSB	E11	Standby +3V (for ATX-style)
+3.3V	D13, D16, D19, D22, D25	+3.3 volt power
VBAT	E9	Battery Backup Supply 3.3V
Ground	E24, D10, D40, C3, C6, C9, C12, C16, C20, C23, C26, C29, C32, C35, B1, B4, B7, B10, B13, B16, B19, B22, B25, B31, B34, B37, B40, A3, A9, A12, A18, A21, A27, A30, A33, A36, A39	Ground

Note: Ground is also present when the card present signal is asserted by I/O cards that support PCI Express. This ground aids in preventing cross talk on adjacent signal pairs.

Reserved Pins

Signal Name	Pin #	Description
Reserved	E10, E32, F15, F16, F23, F27, F28, F29, F30, F31, F32, F33, F34, F35, F36, F37, F38, F39, F40	Reserved for future use, Do Not Connect

3.4 COMIT Connector Physical Specifications

Materials	Spec
Housing:	LCP (Liquid Crystal Polymer) Thermoplastic, UL Rated 94-V0
Contact:	Copper Alloy
RoHS Compliant:	Yes

Contact Finish	Spec
Socket Interface:	30 micro-inches Gold On Contact Area
Terminal Interface:	30 micro-inches Gold On Contact Area
Underplate:	50 micro-inches Minimum of Nickel

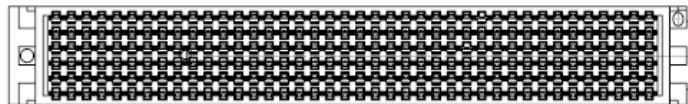
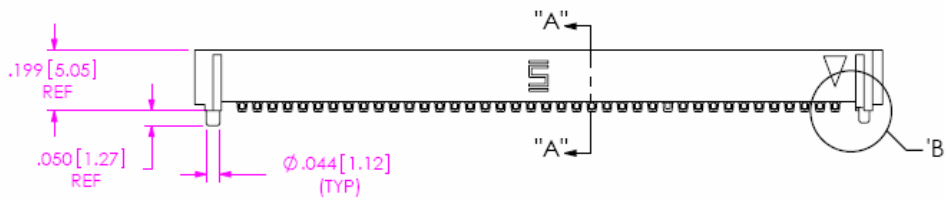
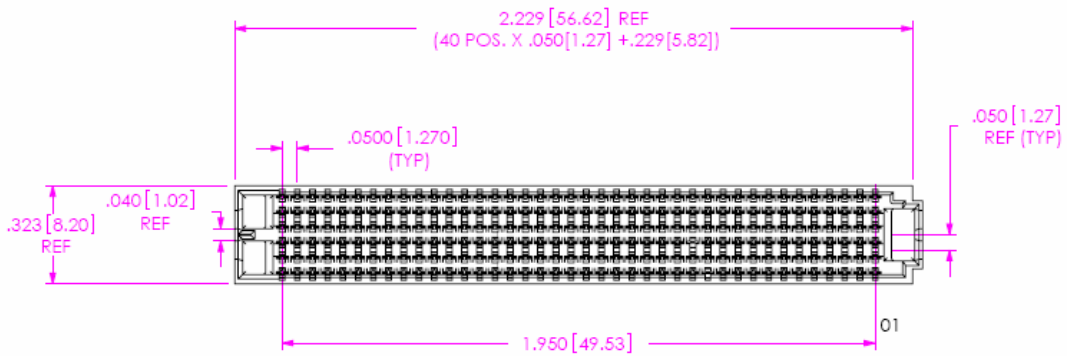
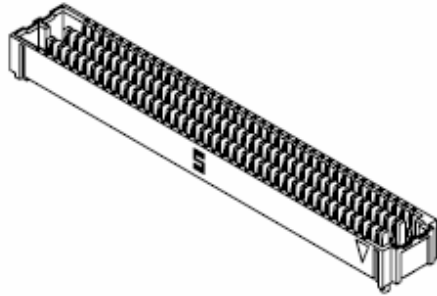
Mechanical Performance	Spec
Insertion Force:	14.7 lbs. maximum
Withdrawal Force	18.9 lbs. minimum
Normal Force:	63 gr. @ 0.009 Inches Deflection
Durability:	500 mating/un-mating Cycles
Operating Temp:	-55°C to +125°C

Electrical Performance	Spec
Contact Resistance:	6.9 milliohms max.
Contact Current Capacity:	2.9 Amps @ 30°C Temp Rise
Dielectric Strength:	900 VAC
Insulation Resistance:	25,000 Meg Ohms Minimum

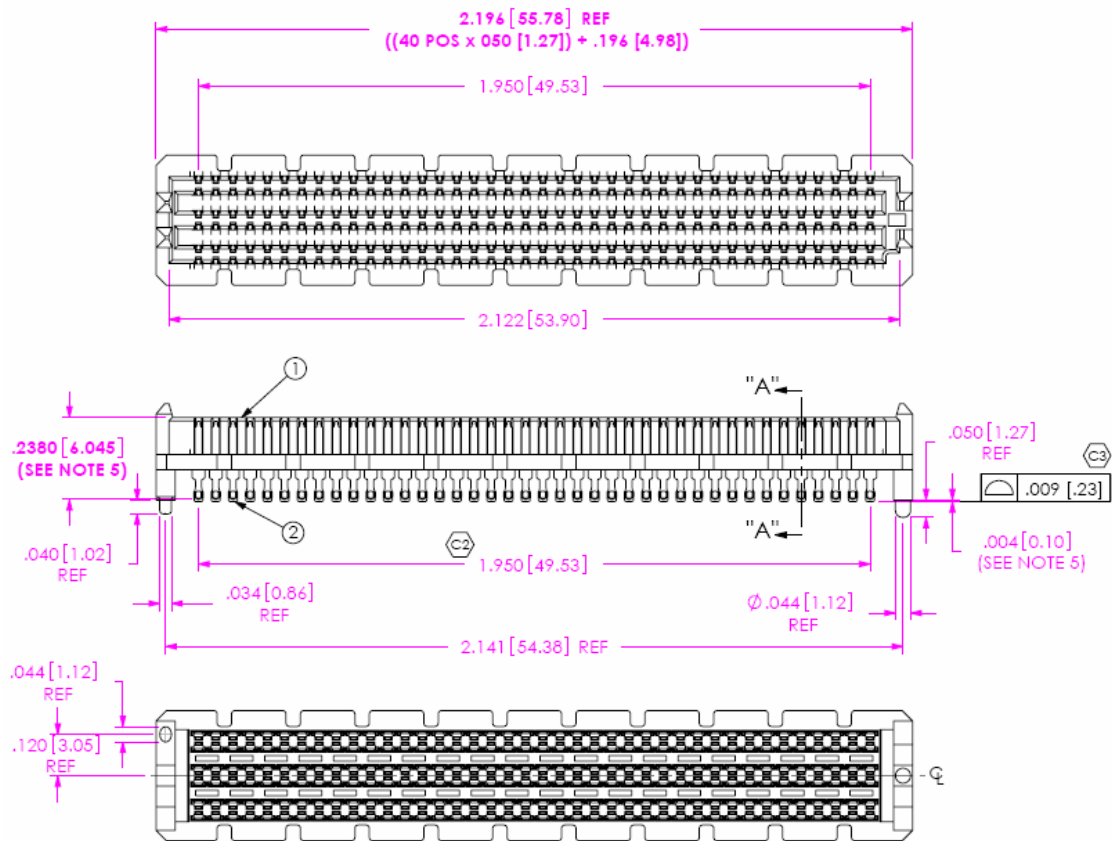
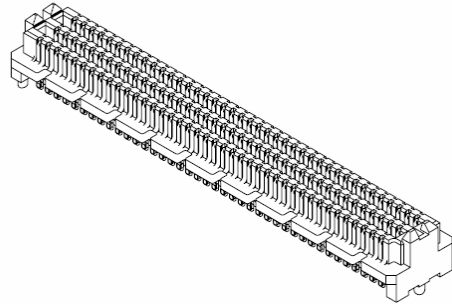
Solderability	Spec
Processing Temperature:	260°C Produces No Blistering, Distortion, or Discoloration

High Frequency Performance	Spec
Single-Ended System Impedance:	50 Ohms ±10%
Differential Pair System Impedance:	100 Ohms ±10%
Differential Performance:	9 GHz differential @ -3db insertion loss

3.5 SEAF Connector Drawings



3.6 SEAM Connector Drawings



3.7 Auxiliary PATA Connector

3.7.1 Rugged 2mm Board-to-Board Connectors

An auxiliary connector for PATA on COMIT has been defined that compliments the main COMIT connector and provides for parallel ATA interface drives to be connected. This connector is optional and may not be included on all implementations.

The TW (processor module) and SMM (baseboard) connector series from Samtec are specified for use with or without standoffs. The mated height of the connector pair is 8.5mm without standoffs, 8.65mm with standoffs.

TW: ASP-140306-03

SMM: ASP-142677-02



The TW and SMM 2mm Connectors from Samtec

The TW standard part number is ASP-140306-03 (Std. Part: TW-22-XX-S-D-195-SM--A--P) and the SMM standard part number is ASP-142677-02 (Std. Part : SMM-122-02-S-D-LC—P A) <http://www.samtec.com/search/comit.aspx>.

The 8.65mm standoff part number from Samtec is ASP-144136-01.
<http://www.samtec.com/search/comit.aspx>

3.7.2 Connector Placement

The TW series 2mm pin header is the PATA connector on the processor module and the SMM rugged 2mm socket is the PATA baseboard connector for COMIT-based boards.

This specification does not address the location (placement) requirements for any specific form factor. Please refer to the separate form factor specifications for detailed COMIT connector placement information.

3.8 PATA Connector Pin Assignments

The PATA auxiliary connector for COMIT conforms to industry standard 2.5", 2mm 44-pin PATA connector pin out.

3.8.1 PATA Connector Signal Descriptions

PCI Express

Signal Name	Pin #	Description
DD0	17	PATA Data 0
DD1	15	PATA Data 1
DD2	13	PATA Data 2
DD3	11	PATA Data 3
DD4	9	PATA Data 4
DD5	7	PATA Data 5
DD6	5	PATA Data 6
DD7	3	PATA Data 7
DD8	4	PATA Data 8
DD9	6	PATA Data 9
DD10	8	PATA Data 10
DD11	10	PATA Data 11
DD12	12	PATA Data 12
DD13	14	PATA Data 13
DD14	16	PATA Data 14
DD15	18	PATA Data 15
DA0	35	PATA Address 0
DA1	33	PATA Address 1
DA2	36	PATA Address 2
CS0#	37	PATA Chip Select 0
CS1#	38	PATA Chip Select 1
IRTRQ	31	Interrupt Request
IOR	25	IO Read
IOW	23	IO Write
IORDY	27	IO Ready
IOCS16	32	(obsolete, now Reserved)
DMARQ	21	DMA Request
DMACK#	29	DMA Acknowledge
CSEL	28	Cable Select
DASP#	39	Device Active
PDIAG#/CBLID#	34	Passed Diag/Cable Identifier
RST#	1	Reset
+5V	41,42	Power
GND	2, 19, 22, 24, 26, 30, 40, 43	Ground
NC	20	No Connect
RESERVED	44	Reserved

3.8.2 PATA Connector Specifications

Materials	Spec
Housing:	LCP (Liquid Crystal Polymer) Thermoplastic, UL Rated 94-V0
Contact:	Phosphor Bronze/ BeCu
RoHS Compliant:	Yes

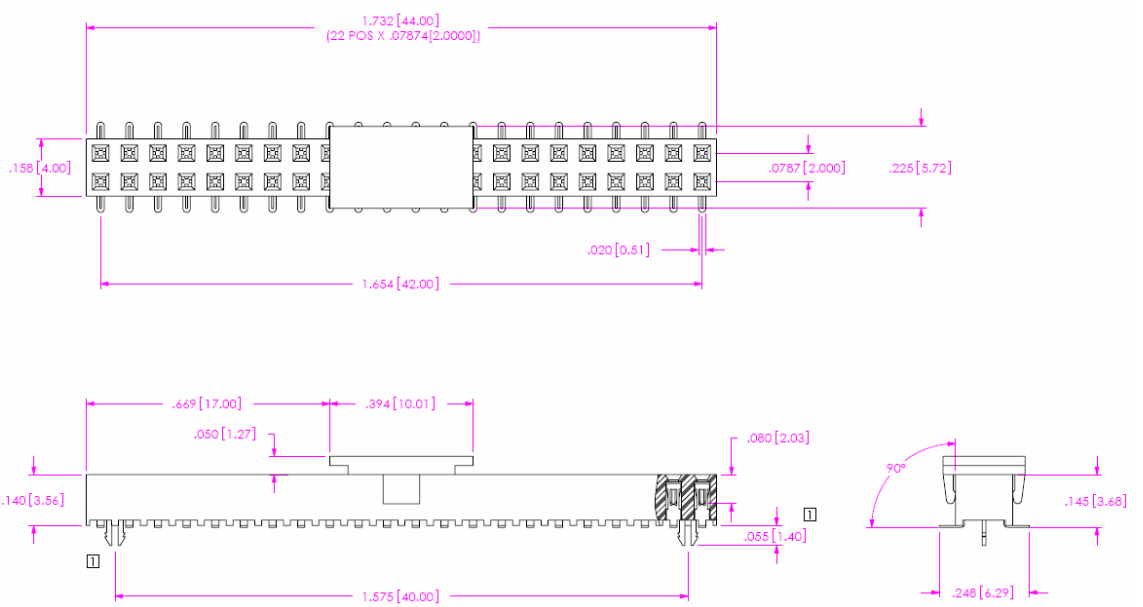
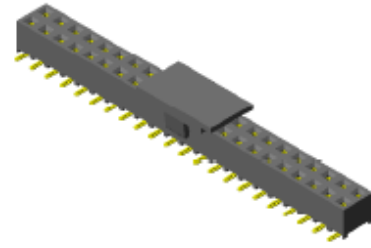
Contact Finish	Spec
Socket Interface:	30 micro-inches Gold On Contact Area
Terminal Interface:	30 micro-inches Gold On Contact Area
Underplate:	50 micro-inches Minimum of Nickel

Mechanical Performance	Spec
Insertion Force	5.5 lbs. average
Withdrawal Force	4.13 lbs. average
Durability:	1000 mating/un-mating cycles
Operating Temp:	-55°C to +125°C

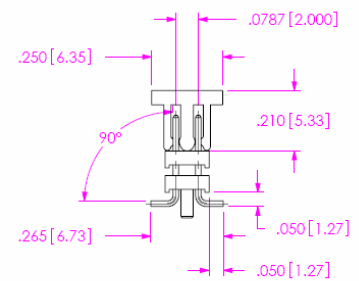
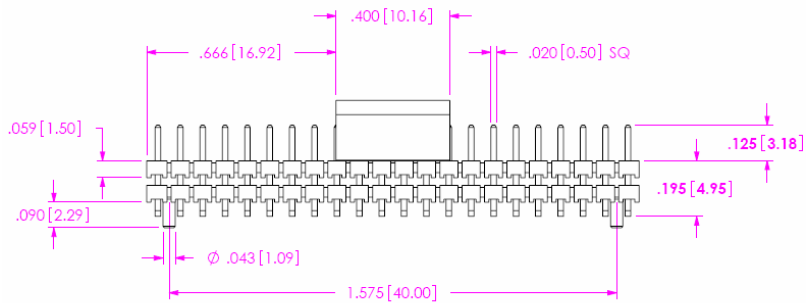
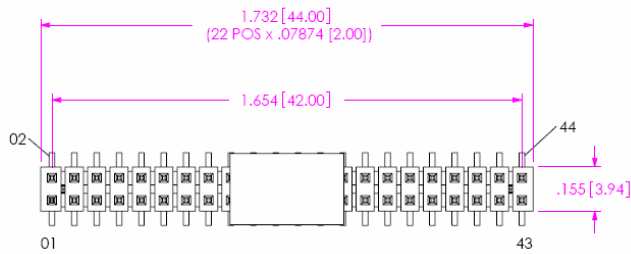
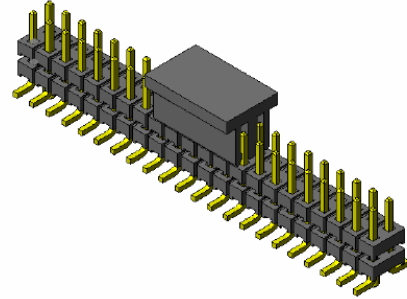
Electrical Performance	Spec
Contact Resistance:	10 milliohms max.
Contact Current Capacity:	3.0Amps @ 30°C Temp Rise
Dielectric Strength:	1000 VAC
Insulation Resistance:	5,000 Meg Ohms Minimum

Solderability	Spec
Processing Temperature:	260°C Produces No Blistering, Distortion, or Discoloration

3.8.3 PATA SMM Connector Drawings for use on a Baseboard



3.8.4 PATA TW Connector Drawings for use on the COMIT Processor Module



4.0 Recommended Design Practices

4.1 Implementing COMIT

Products designed with COMIT technology can have multiple, diverse interconnect buses in a single connector. Ultra-high speed, high speed, and moderate-to-low speed interfaces can easily coexist on a single connector with a simple, conservative approach to layout. Considerable effort has been made to ensure that routing on both processor modules and baseboards are efficient. Consideration to design rules and limitations for each respective interface has been given.

The following section is intended to help the designer identify areas for special consideration and further research. This design guideline should by no means be considered a complete reference, only a reasonable starting point. Following these guidelines does not guarantee a successful design. There are many sources available that discuss high-speed printed circuit board design, USB, or PCI Express specific design guidelines. The following is no way an attempt to repeat this information or instruct the designer in these areas. It merely touches on general guidelines that should be observed, as well as some COMIT specific design rules.

Any designer building a processor module, SBC, or an expansion product with COMIT technology should refer to the “Related Documents and Organizations” in Section 1.3 of this Specification for links to applicable specifications and their governing bodies.

4.2 COMIT General Layout Recommendations

Component maximum height is specified to be 5.5mm for the processor module (on the COMIT connector side) and 3.0mm maximum height for the baseboard (again on the COMIT connector side). These specifications apply for the entire area between the two boards to prevent mechanical interference issues when modules are plugged into baseboards.

COMIT supports several common interfaces for low to moderate speed expansion requirements. Industry standard serial interfaces include SMBus, I²C, SPI, Microwire, and a UART. SMBus alert is included for power management alert functionality or general SMBus interrupt usage. Two chip selects are included for SPI/uWire, which can be expanded within the target device to any number needed. SPI and SMBus are defined as 3.3V signaling. Five volt tolerant devices may be used as long as they do not drive the SPI signals on the bus beyond the 3.3V nominal specification. The UART signals are defined as 3.3V only. Level translators must be on the baseboard where needed.

If more bandwidth is required, an LPC bus interface is also available that includes SERIRQ signaling for interrupts and LDRQ for direct memory access transfers. The LPC interface directly provides support for LPC and FWH devices, as well as is the only remaining embedded interconnect solution for support of legacy ISA devices on new processor products. A simple bridge chip on the baseboard or a transition board in a SUMIT stack is all that is required for ISA. VGA, HD audio, digital video, LVDS, ENET,

and SDIO interfaces are also included and must conform to industry standard routing and layout guidelines.

Routing for all of these interfaces falls into “best design practice” for standard printed circuit board layout. For more specific information, refer to the parent specification of each interface referenced in Section 1.3, or to data available from the manufacturer for the target device implemented.

COMIT General Layout and Routing considerations

- Signal names on the connector are the context of the processor/chipset. (e.g. SPIDO on the connector is the processor/chipset’s SPI Interface Data Out pin and should be coupled to the final IO devices corresponding receive input pin)
- The COMIT processor must include all input termination to the module. This includes all control and interface input pull-up or pull-down termination.
- The COMIT processor module must terminate all unused output signals at the connector to ensure features not included on the baseboard are not left floating. (e.g. LVDS_{SEN}, BLE_N, and the LVDS data pairs must be terminated inactive if LVDS is not supported on the processor; USB power enable must be terminated active if the processor module does not include a bit for this function, inactive if unused; no termination required on unused PCIe signals, etc).
- The COMIT processor module must terminate all unused input signals at the connector where necessary to ensure features not included on the base board do not leave inputs floating at the connector to the processor module. (e.g. the baseboard may not support over current on the USB channels, the processor must include a pull up for this pin, no termination required on unused PCIe signals, etc).
- All series termination must be on the processor module. This includes series resistors for PATA, LVDS, etc. This is to minimize inter-compatibility issues when mixing various combinations of processor modules and baseboards.
- Ethernet interfaces on COMIT are specified to include magnetic on the processor module. This mitigates issues with incompatibilities between various vendors and speeds of interfaces and the large choice of magnetic configurations and packages. For most applications, magnetics should be placed on the same side of the processor module as the COMIT connector and adhere to the maximum 5.5mm height specification.
- If unused on the baseboard, 33MHz and 14.31818MHz clock signals should be terminated into a resistor near the COMIT connector. Both of these signals are specified to drive a maximum of two loads.
- 33MHz and 14.31818MHz clocks must be stable a minimum of 3 mS before PERST goes inactive. This is to allow clock buffers on the base board to stabilize with chipsets that gate these signals.
- PWRGOOD, RSTBTN#, PWRBTN#, SMI, and WAKE# must be pulled up to +3.3V on the processor module.
- VBAT is battery backup for CMOS clock and low power non-volatile static RAM. It is specified as 3.3V and must include diode-OR function on baseboard.

4.3 COMIT USB Routing Recommendations

COMIT supports six USB signal pairs routed through the connector. Also, one overcurrent and one enable signal for the six ports (wire OR) are included in the same connector. Overcurrent is a 3.3V compatible signal and shall have termination included on the processor module.

With a -3dB differential bandwidth specification at 9 GHz, COMIT is USB speed independent. As of the release of this specification, all speeds of USB signaling are compatible with the connectors used in COMIT. Both the manufacturer of the COMIT connected USB host card and the baseboard or SUMIT connected USB target must design to the respective specifications of the device used. USB OTG (On-The-Go) compatible and USB slave devices may also be implemented with COMIT because a USB client detect signal is included in the connector.

General routing recommendations and considerations for USB are commonly available. COMIT specific implementations only need to ensure that these are met, and to observe the recommendations below.

Recommended USB Implementation Guidelines:

- COMIT specifies that USB power switches NOT be located on the COMIT processor module unless the USB device connects directly to the processor module itself. Use USB specific, active power switching devices located directly at the device or connector leading off of the baseboard or SUMIT card. The use of polyfuse type protection circuitry is acceptable but less desirable than active switches in embedded systems because of the fast acting and in-rush limiting qualities of active devices. Omitting protection for baseboard or SUMIT device connections is strongly discouraged.
- For designers of devices that consume more than 500 mA @5V continuous, refer to Section 4.5 and to the specific COMIT enabled baseboard specifications for system power considerations.
- Ample bypassing and bulk decoupling at the switches on the baseboard is mandatory to prevent system brown out or reset issues during USB hot swap device insertion or power up.

4.4 COMIT PCI Express Routing Recommendations

COMIT supports PCI Express signaling. Three x1 and a single x4 links are supported in the connector. Optionally, the x4 link can be divided into up to four additional x1 links for a total of seven PCIe x1 links. One Card Present for each link, a separate clock pair for each link (only 1 clock pair is provided for the x4 link whether used as a single link or as four separate x1 links), and one common Wake signal is included in the pin definition for COMIT.

PCI Express requires careful consideration when laying out a processor or I/O expansion board. PCI Express Generation 1 is a 1.25 Gigabit per second differential serial interface. With a maximum edge rate specified at 50 picoseconds, or 7 GHz, routing is critical. Even at realized edge rates of ~100 picoseconds, attention to detail is required for a successful design.

When designing a printed circuit board for any extremely high-speed differential signaling environment, the symmetry of the circuit is of utmost importance. Matching each segment pair length, matching left hand and right hand turns for the pair, placing vias or components symmetrically in the signal path, and routing the trace pair symmetrically to these features are critical to minimize impedance, reflection, and flight time mismatches that degrade signal quality at these frequencies.

Recommended PCI Express Implementation Guidelines:

- Signal names on the connector are from the context of the processor/chipset. This is consistent with the PCI Express specification. (e.g. PETp0 on the connector is the processor board's PCIe transmit positive pin and should be coupled to the I/O device's corresponding PCIe receive pin)
- 100 ohms \pm 20% characteristic differential impedance
- 0.020" minimum space from differential pairs to adjacent conductors
- Match signals of differential pair as closely as possible, 0.005" max per board
- One via per card per signal plus one via each end for breakout
- Vias placed symmetrically in the differential pair path
- Capacitive coupling components placed as close as possible to transmitter and placed symmetrically in the differential pair trace path
- Match number of turns left and right, no sharp or 90 degree turns
- Microstrip routing only over solid planes. (No routing over breaks in planes)
- Stripline routing is not recommended unless using blind or back drilled vias to eliminate the stub
- Match lane to lane length within a link to \pm 0.50" on COMIT processor module, \pm 2.00" on baseboard and \pm 0.50" on an expansion card
- Maximum lane length on a processor module is 4.00" component to connector (assumes FR4 type dielectric for loss and jitter budget)
- Maximum lane length on a SBC is 10.00" connector to component or connector (assumes FR4 type dielectric for loss and jitter budget)
- Maximum lane length on an expansion card is 2.50" connector to component (assumes FR4 type dielectric for loss and jitter budget)
- Card present signals are grounded by the target device/card for the link(s) consumed only.

4.5 COMIT Power

The COMIT Specification provides for ample power through the connector. Power is supplied to the processor module through the COMIT connector on designated pins. It is highly recommended that switching type power supplies be used to generate processor module voltages necessary because of their excellent transient response and their inherently high efficiency.

4.5.1 COMIT Power Sequencing

The COMIT Specification power sequencing requirements are defined to ensure module reliability and cross-compatibility performance.

Start-up Power Sequence Requirements:

- VBAT must come up at the same time or before +5VSB comes up
- +5VSB must come up at the same time or before +3.3VSB comes up
- +3.3VSB must come up at the same time or before +5V comes up
- +5V must come up at the same time or before +3.3V comes up
- ALLSYS_PWRGOOD must be active at the same time or after +3.3V comes up

Stop Power Sequence Requirements:

- ALLSYS_PWRGOOD must be inactive at the same time or before +3.3V goes down
- +3.3V must go down at the same time or before +5V goes down
- +5V must go down at the same time or before +3.3VSB goes down
- +3.3VSB must go down at the same time or before +5VSB goes down
- +5VSB must go down at the same time or before VBAT goes down

4.5.2 COMIT Minimum Power

The COMIT Specification does not specify the minimum power requirement a baseboard must provide to processor modules. This will be specified within each standard form-factor mechanical specification to support the unique minimum requirements of each size module. Please see the individual mechanical form-factor specification for more information.

4.5.3 COMIT Maximum Power

Ample current carrying capacity is available from the COMIT connector for a wide variety of applications and processors. The power available to the COMIT processor module from the chosen baseboard solution must be specified by the vendor for the baseboard. These limits may differ significantly from the total power available defined in the chart below as a maximum of this specification. Power requirements in excess of the baseboard available power specification, or greater than those listed below for the COMIT connector capability, must be supplied by a secondary connector on the processor module itself. Baseboard available power to the processor module will vary from vendor to vendor, please consult the manufacturer's documentation.

The following table describes the maximum continuous power available from the COMIT connector for the processor module.

COMIT Connector Power Specifications

COMIT Connector Maximum Power:	
+5V	20 Amps continuous
+5VSB	4 Amps continuous
+3VSB	2 Amps continuous
+3.3V	10 Amps continuous
VBAT	2 Amps continuous

4.5.4 COMIT Operating Power Modes

The following table describes the various modes in which power to the module is enabled.

COMIT Connector Baseboard Power Modes

Power Rail	S0	S3	S4	S5	Notes:
+5V	ON	OFF	OFF	OFF	Disable is SLP_S3# = 0
+3.3V	ON	OFF	OFF	OFF	Disable is SLP_S3# = 0
+5VSB	ON	ON	ON	ON	Always on
+3VSB	ON	ON	ON	ON	Always on
VBAT	ON	ON	ON	ON	Battery for CMOS and RTC backup

5.0 Name and Logo Use

The use of the COMIT logo is a privilege granted by the SFF-SIG to member companies who believe their products comply with this Specification. Use of the logo by either members or non-members implies such compliance. The SFF-SIG may revoke permission to use logos if they are misused. The COMIT logo is as follows:



The CMYK colors are:		<u>C</u>	<u>M</u>	<u>Y</u>	<u>K</u>
	Green	55,	0,	100,	0
	Light Blue	37,	7,	3,	0
	Orange	0,	74,	100,	0
	Dark Blue	81,	61,	0,	0
	Black	0,	0,	0,	100

The COMIT logo must be printed in black or color. The aspect ratio of the entire logo must be maintained, but the size may be varied. Nothing may be added or deleted from the COMIT logo. Permission is automatically granted to designated SFF-SIG members only as stipulated on the most recent membership agreement during the period of time for which their membership dues are paid.

The COMIT name and logo are trademarks of the Small Form Factor Special Interest Group and must be acknowledged in all published literature and advertising material in all media formats (i.e. print, electronic, web, etc.).